#4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No. 035905/0104

In re patent application of
Thomas H. LEE et al.
Serial No. 09/927,648 Art Unit: 2818
Filed: August 13, 2001 Examiner: Unassigned
For: DENSE ARRAYS AND CHARGE STORAGE DEVICES, AND METHODS FOR MAKING SAME

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

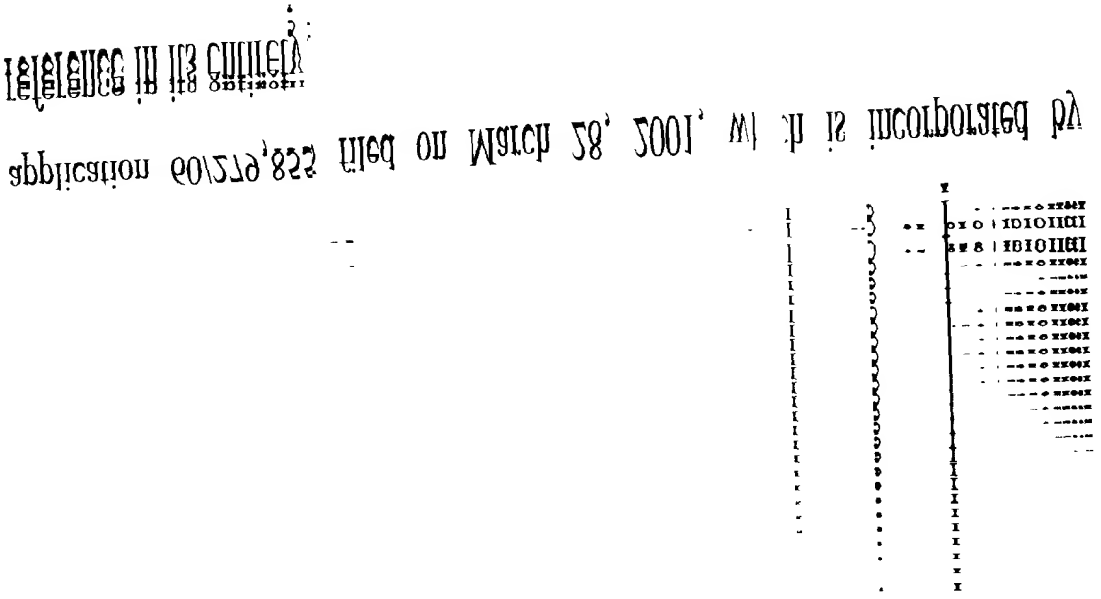
Prior to the first Office Action on the merits, please amend the application as follows:

In the Specification:

Please amend Page 1 of the specification by replacing the first paragraph after the Title with the following paragraph:

This application is a continuation-in-part of U.S. Application Serial Number 09/801,233, filed on March 6, 2001, which is a continuation-in-part of U.S. Application Serial Number 09/745,125, filed on December 21, 2000, both of which are incorporated by reference in their entirety. This application is also a continuation-in-part of U.S. Application Serial Number 09/639,579 filed on August 14, 2000, which is incorporated by reference in its entirety. This application is also a continuation-in-part of U.S. Application Serial Number 09/639,702 filed on August 14, 2000, which is incorporated by reference in its

entirety. This application is also a continuation-in-part of U.S. Application Serial Number 09/639,749 filed on August 17, 2000, which is incorporated by reference in its entirety. This application also claims benefit of priority of provisional application 60/279,855 filed on March 28, 2001, which is incorporated by reference in its entirety.



application 60/279,855 filed on March 28, 2001, which is incorporated by reference in its entirety.

entirety. This application is also a continuation-in-part of .S. Application Serial Number 09/639,749 filed on August 17, 2000, which is in› rporated by reference in its entirety. This application also claims benefit of riority of provisional application 60/279,855 filed on March 28, 2001, whi › is incorporated by reference in its entirety.

REMARKS

The Preliminary Amendment is submitted to correc the filing dates of two priority applications Serial Number 09/745,125 and 09/63' 749 provided on page 1, paragraph 1 of the application, such that these filing ates correspond to the filing dates officially granted to these priority application by the USPTO. The corrected filing dates of these two priority applications lso correspond to the filing dates noted for these applications on the Filing Recei mailed September 14, 2001.

Should there be any questions concerning this appl ation, the Examiner is invited to contact the undersigned at the number listed belo

Respect lly submitted,

11/14/01
Date

Leon Rado sky
Reg. No. 4 .445

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Washington, D.C. 20007-5109
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Fax: (202) 672-5399

THE COMMISSIONER IS HEREBY AUTHORIZED TO CHARGE ANY DI ICIENCY OR CREDIT ANY OVERPAYMENT TO DEPOSIT ACCOUNT NO. 19-0741.

Redlined Version of the Amendment to Show C anges Made

This application is a continuation-in-part of U.S. App cation Serial Number 09/801,233, filed on March 6, 2001, which is a conti uation-in-part of U.S. Application Serial Number 09/745,125, filed on Decembe 21 [22], 2000, both of which are incorporated by reference in their entirety. Th s application is also a continuation-in-part of U.S. Application Serial Numbe 09/639,579 filed on August 14, 2000, which is incorporated by reference n its entirety. This application is also a continuation-in-part of U.S. App cation Serial Number 09/639,702 filed on August 14, 2000, which is incorpor ed by reference in its entirety. This application is also a continuation-in-part of U.S. Application Serial Number 09/639,749 filed on August 17 [14], 2000, wh ch is incorporated by reference in its entirety. This application also claims benefit of priority of provisional application 60/279,855 filed on March 28, 200 which is incorporated by reference in its entirety.

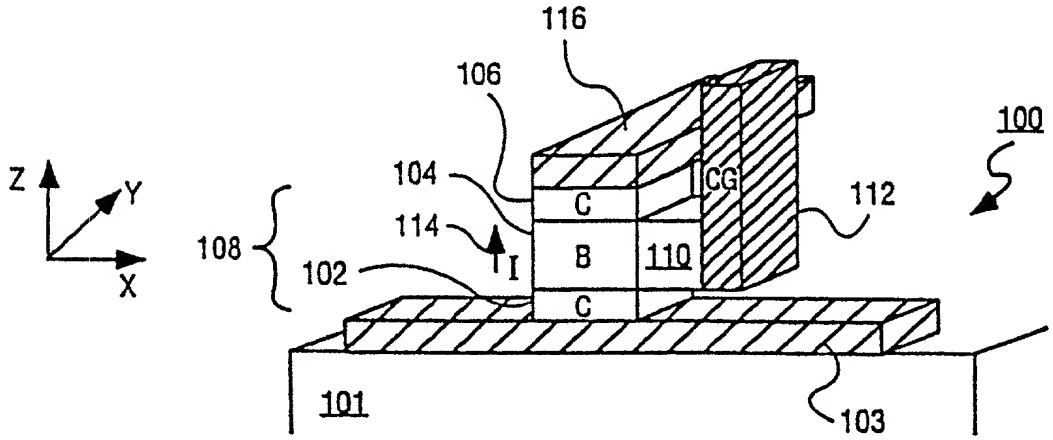

FIG. 1A

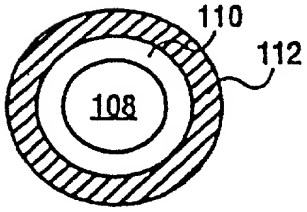

FIG. 1B

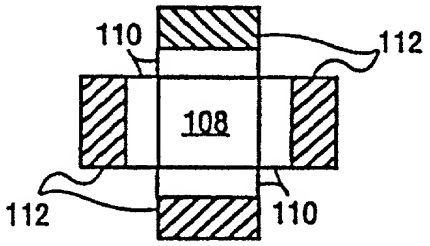

FIG. 1C

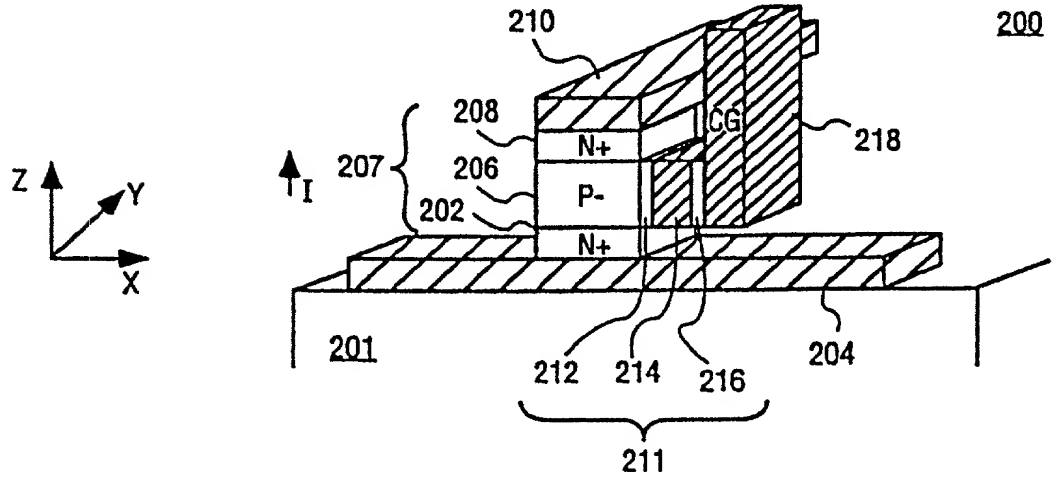

FIG. 2

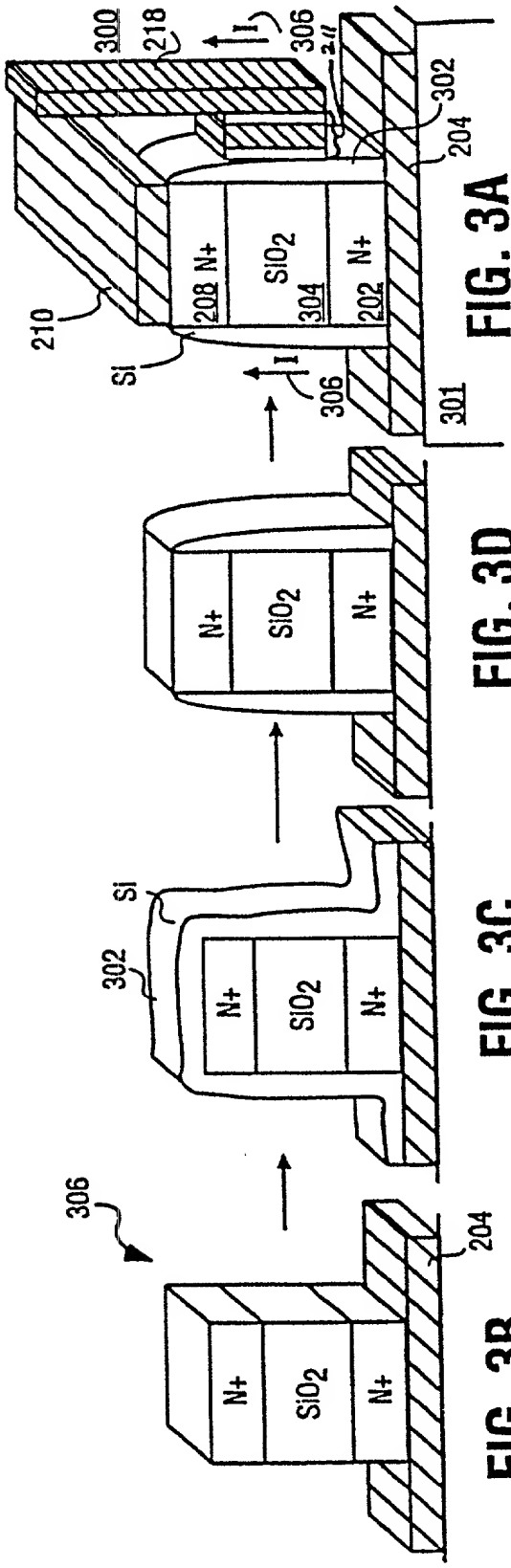

FIG. 3A

FIG. 3D

FIG. 3C

FIG. 3B

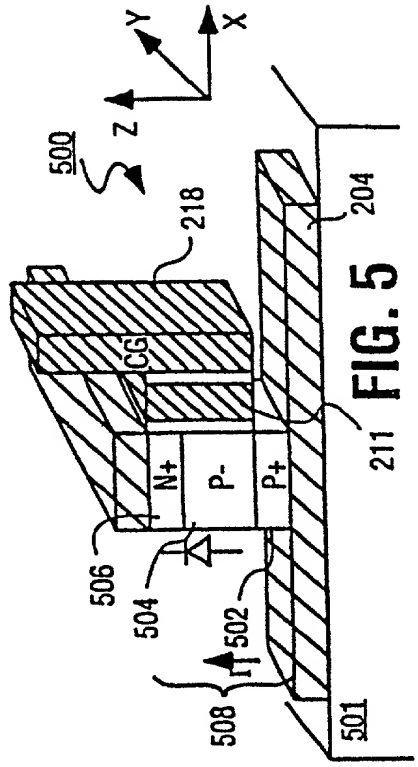

FIG. 5

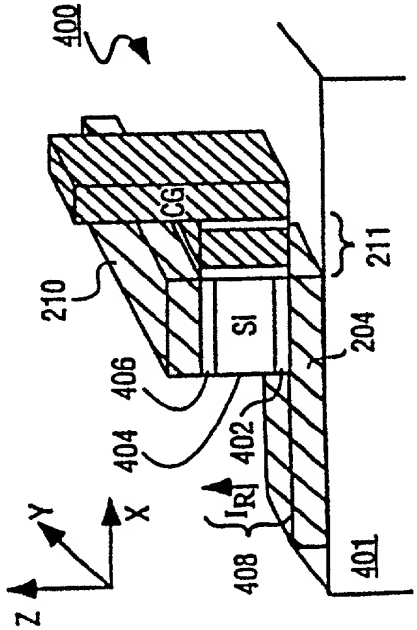

FIG. 4

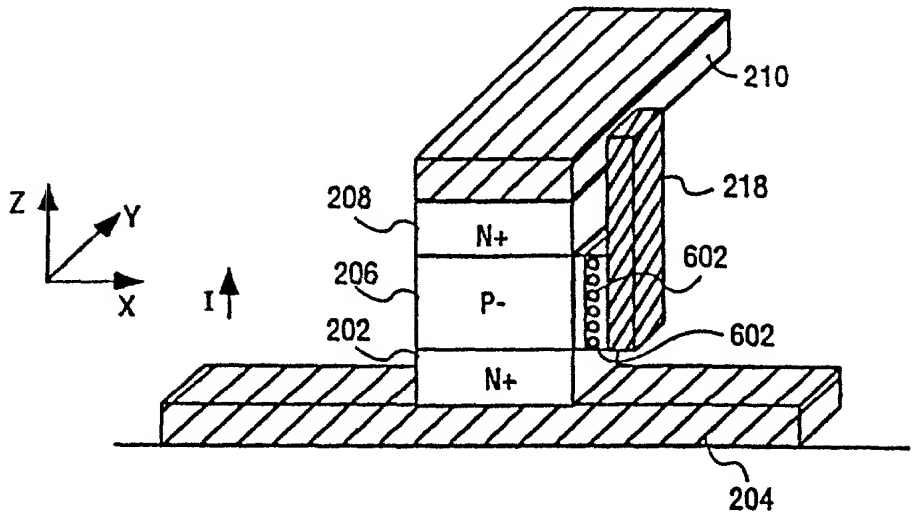
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FIG. 6

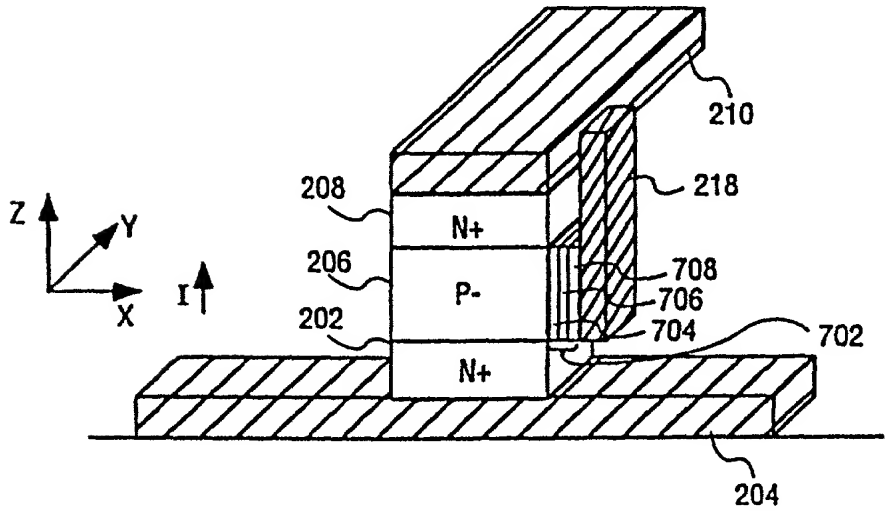
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FIG. 7

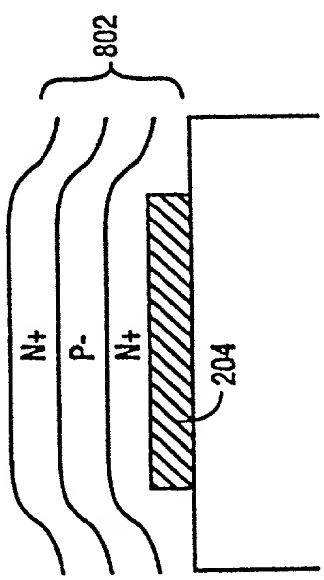


FIG. 8A

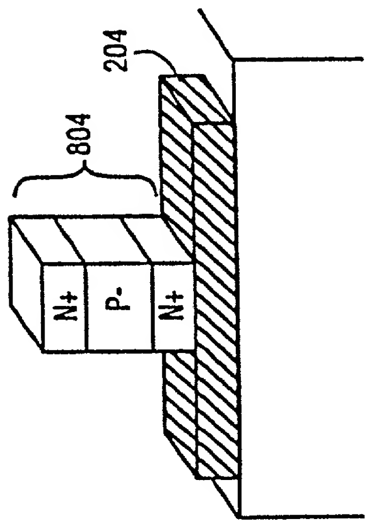


FIG. 8B

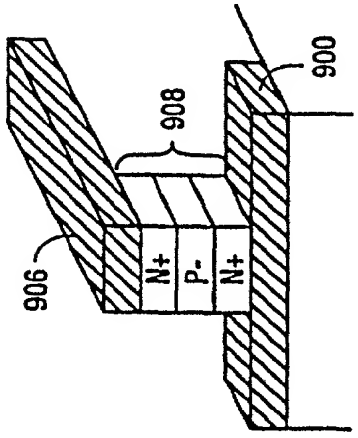


FIG. 9B

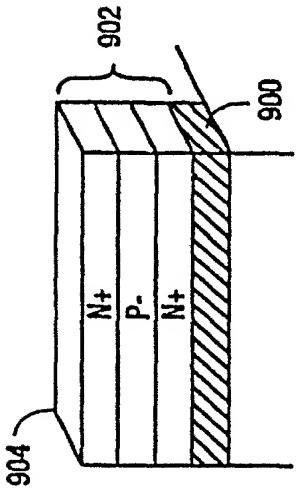


FIG. 9A

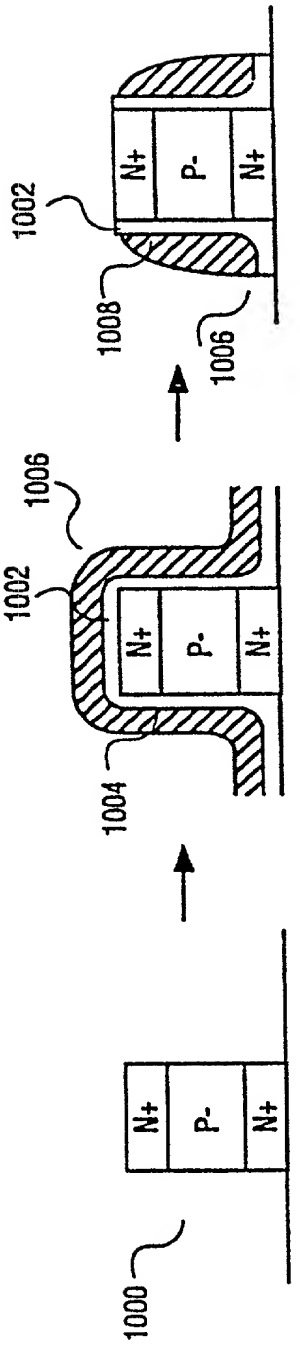


FIG. 10A

FIG. 10B

FIG. 10C

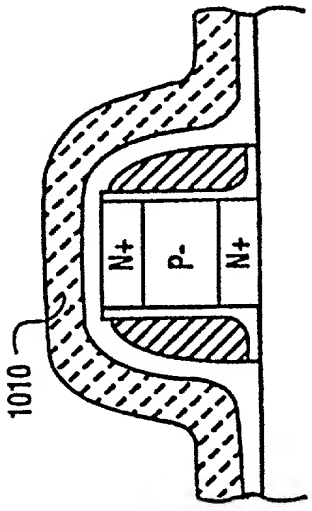


FIG. 10D

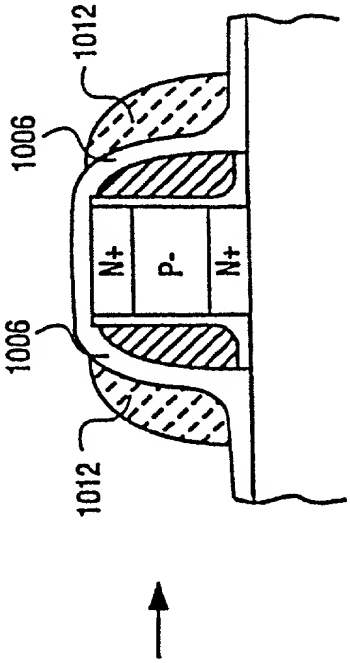


FIG. 10E

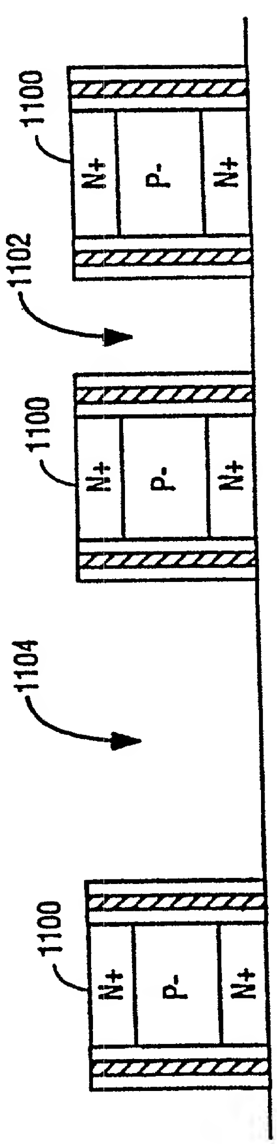


FIG. 11A

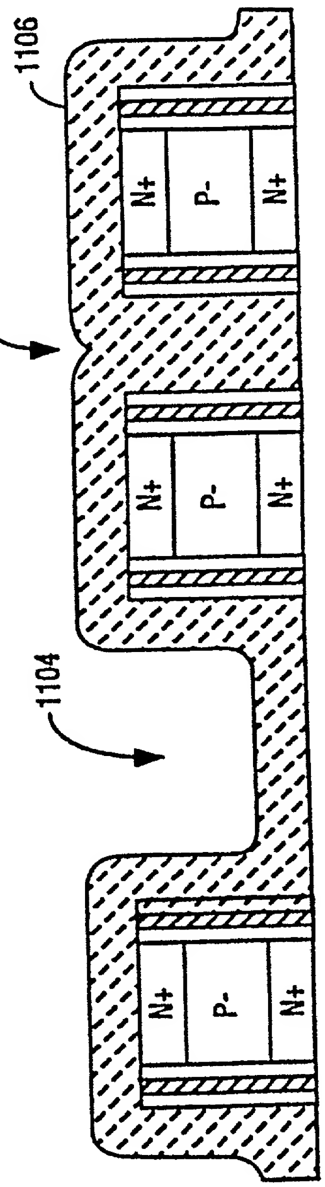


FIG. 11B

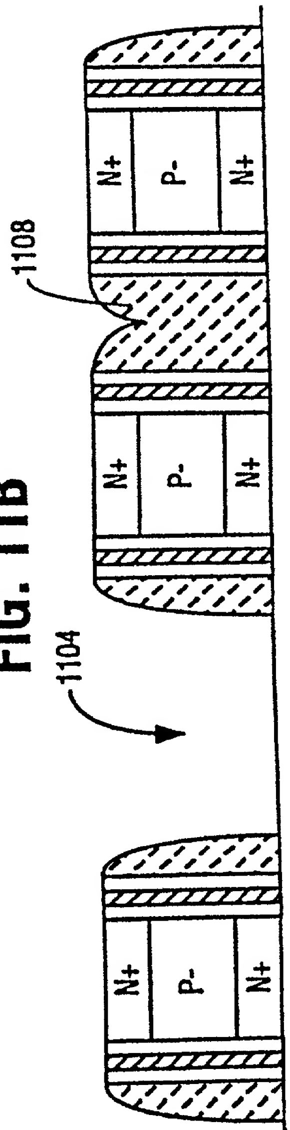


FIG. 11C

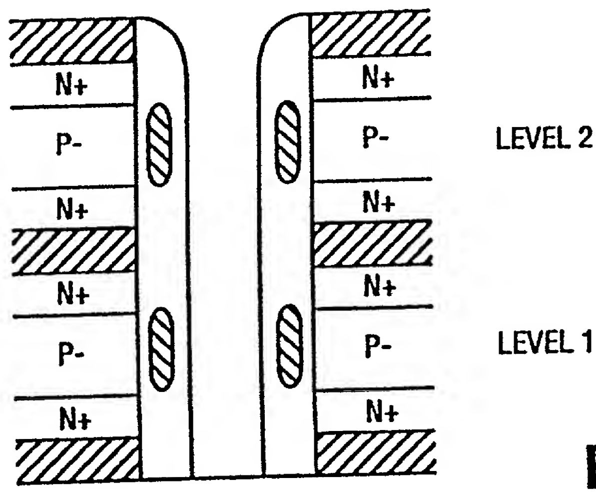


FIG. 12A

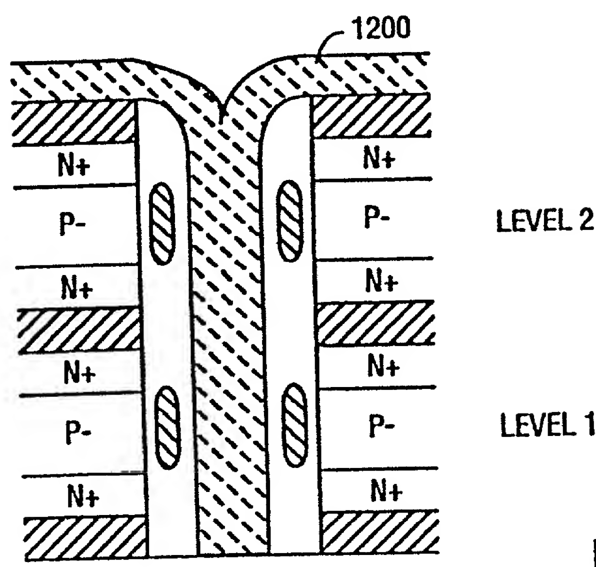


FIG. 12B

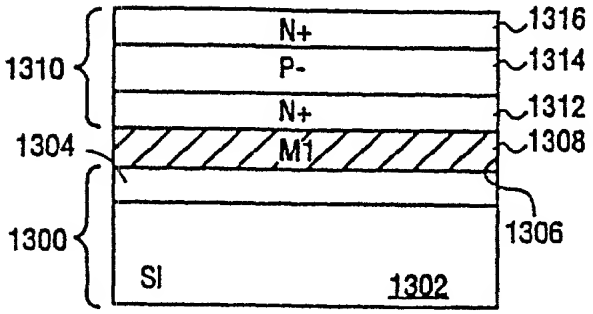


FIG. 13A

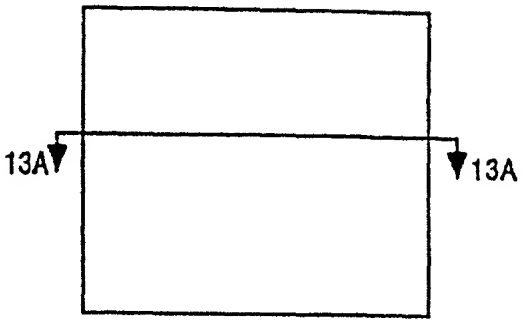


FIG. 13B

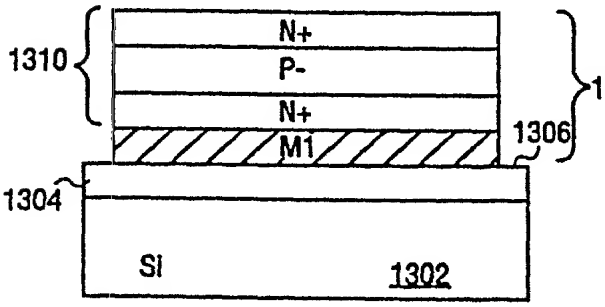


FIG. 14A

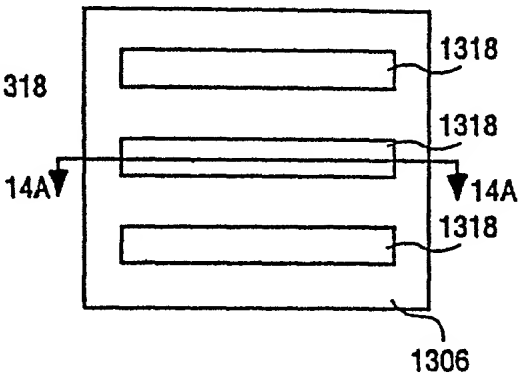


FIG. 14B

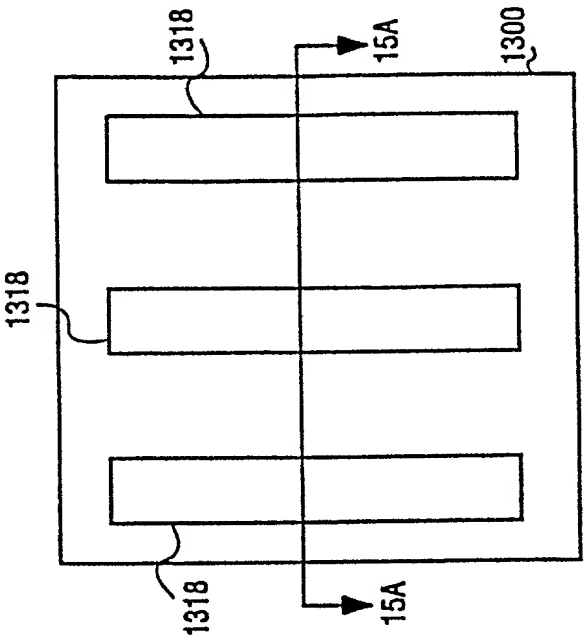


FIG. 15B

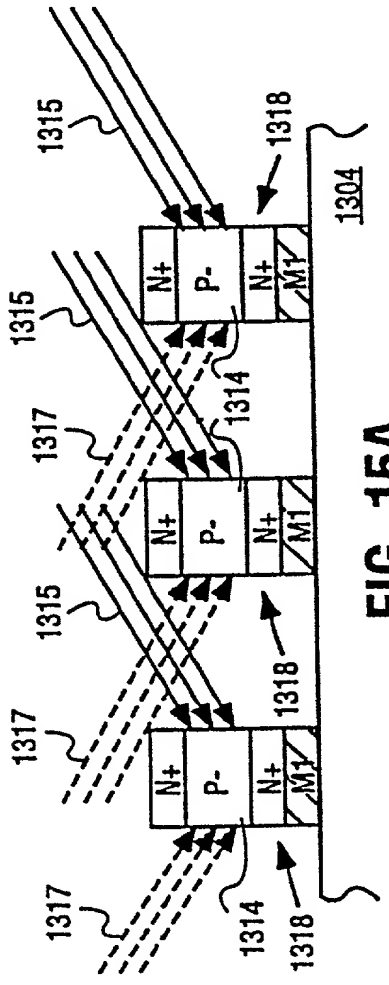


FIG. 15A

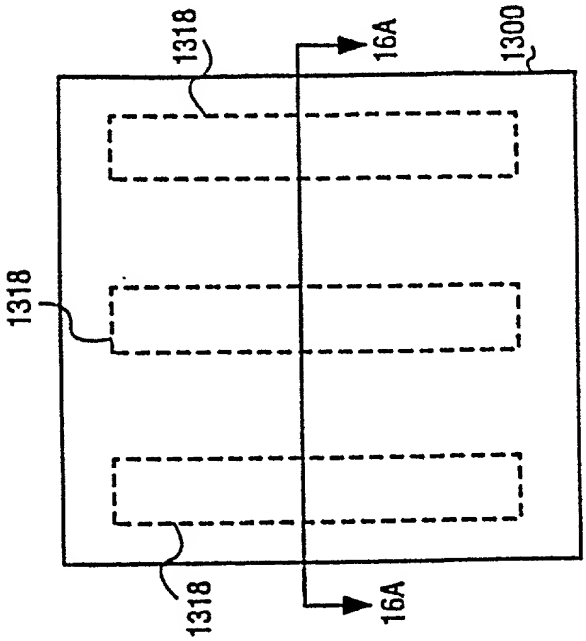


FIG. 16B

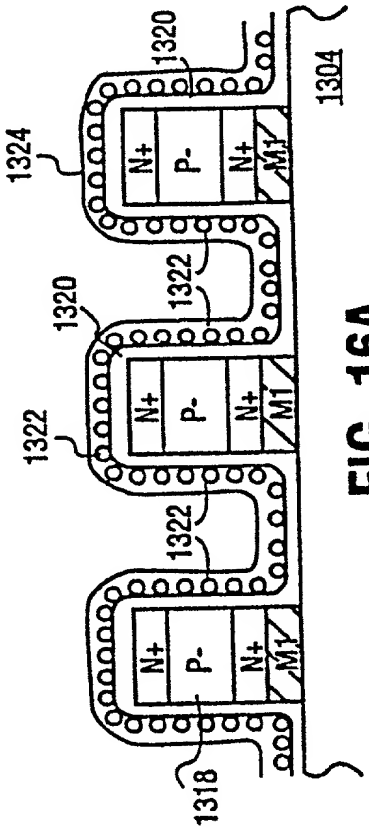


FIG. 16A

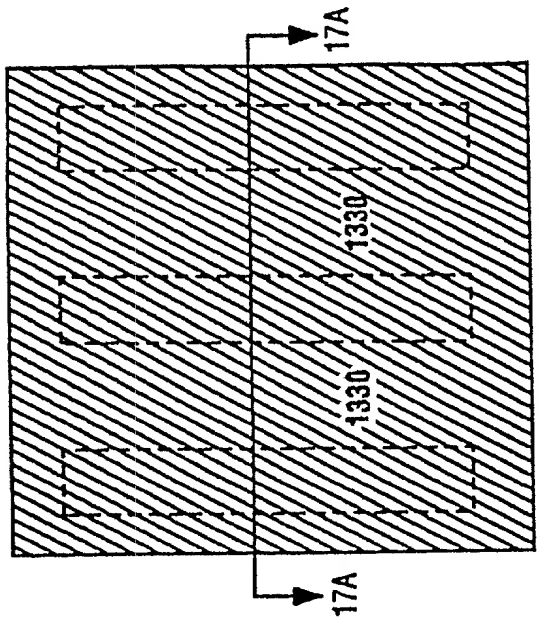


FIG. 17B

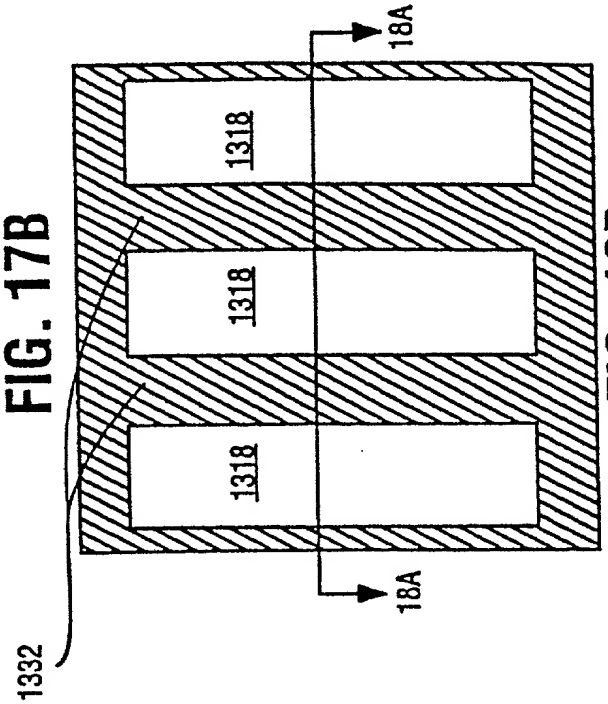


FIG. 18B

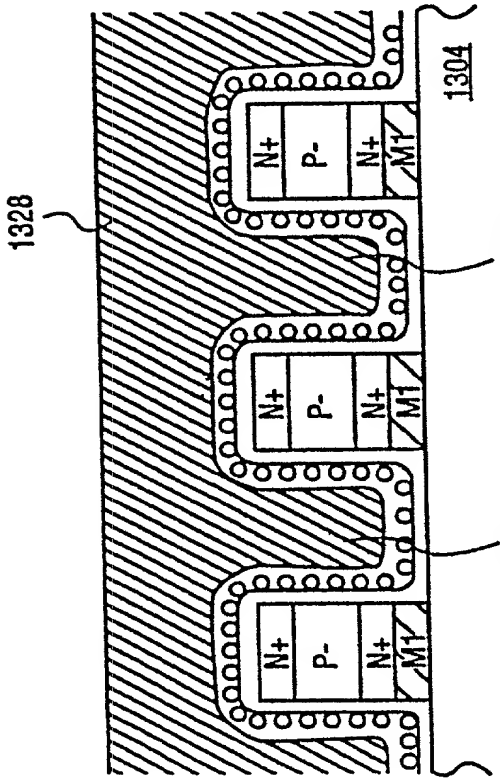


FIG. 17A

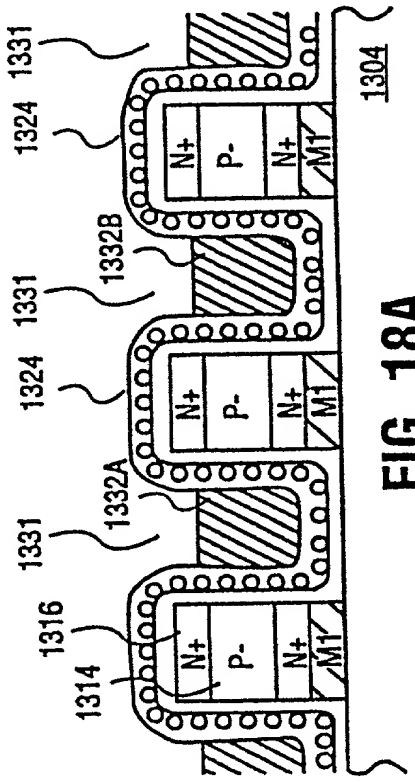


FIG. 18A

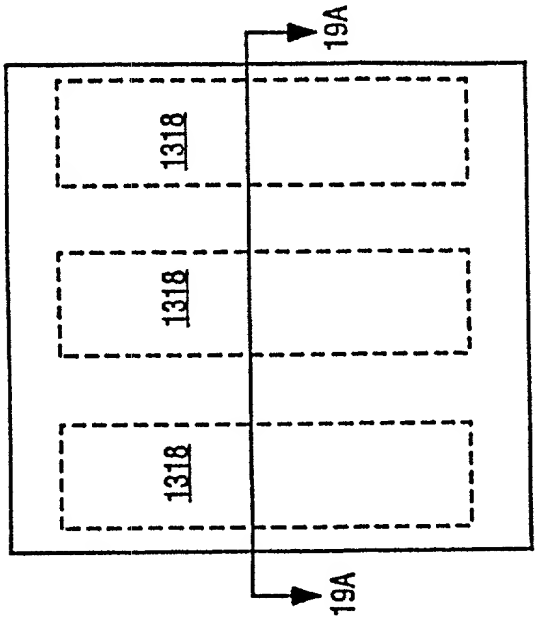


FIG. 19B

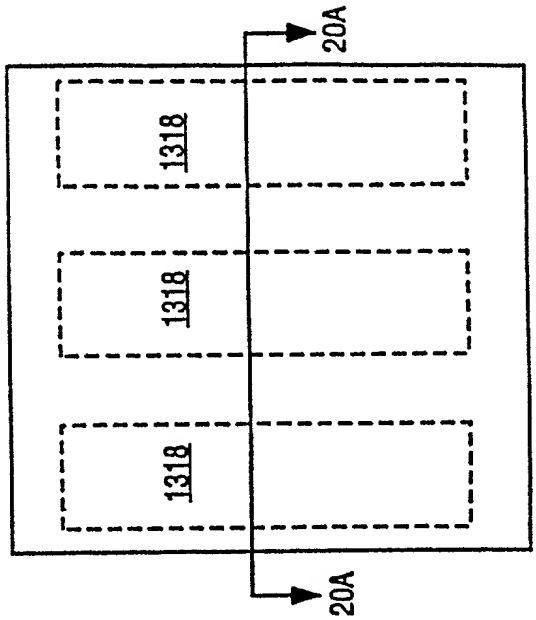


FIG. 20B

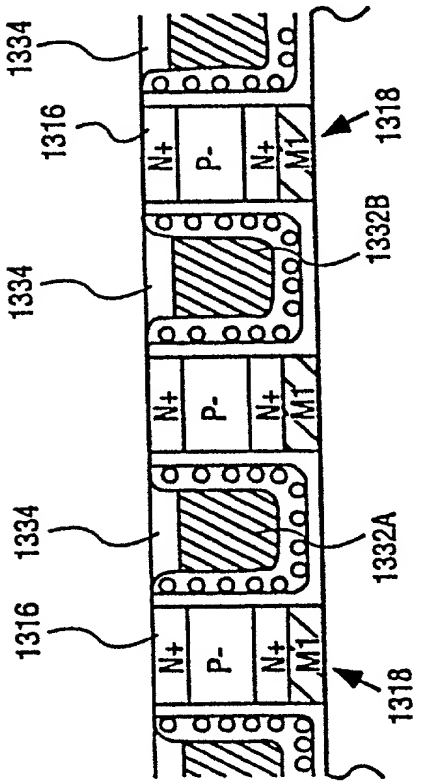


FIG. 19A

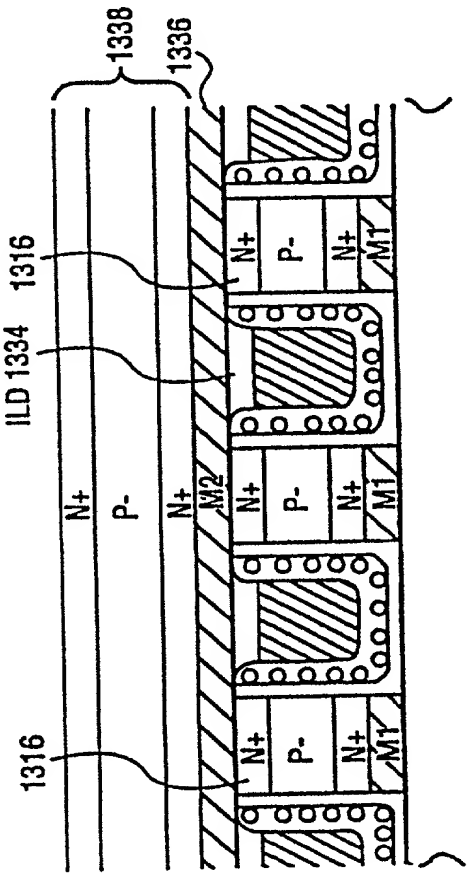


FIG. 20A

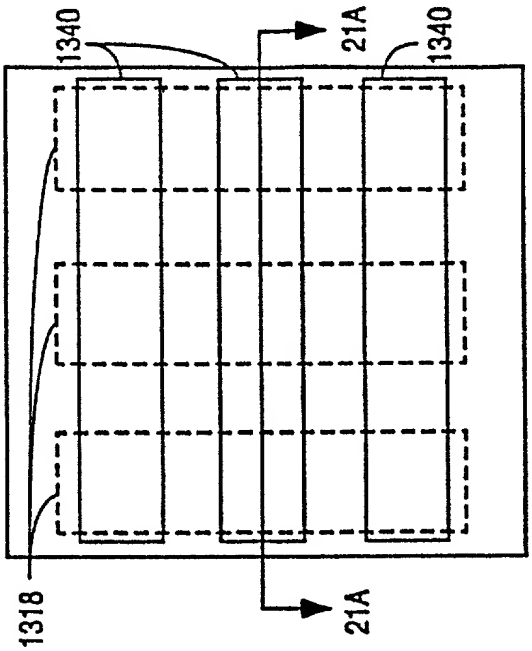


FIG. 21B

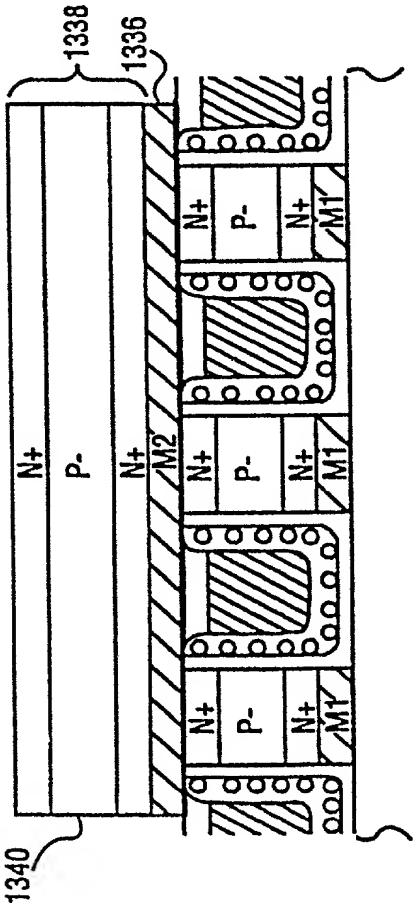


FIG. 21A

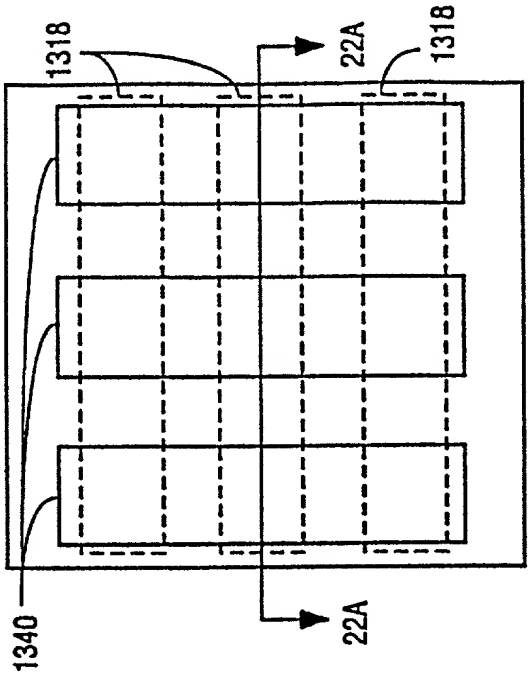


FIG. 22B

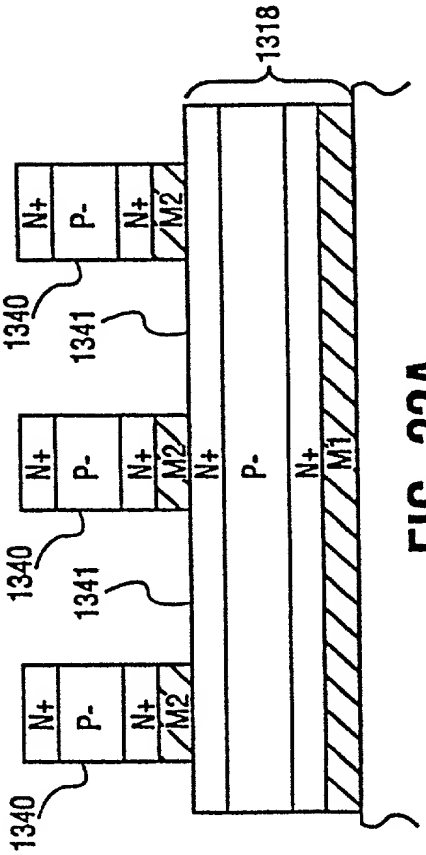


FIG. 22A

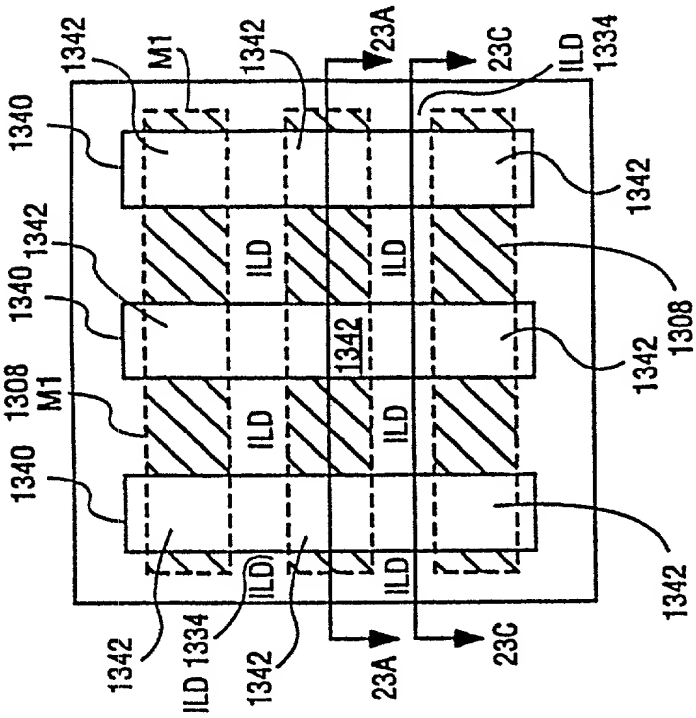


FIG. 23B

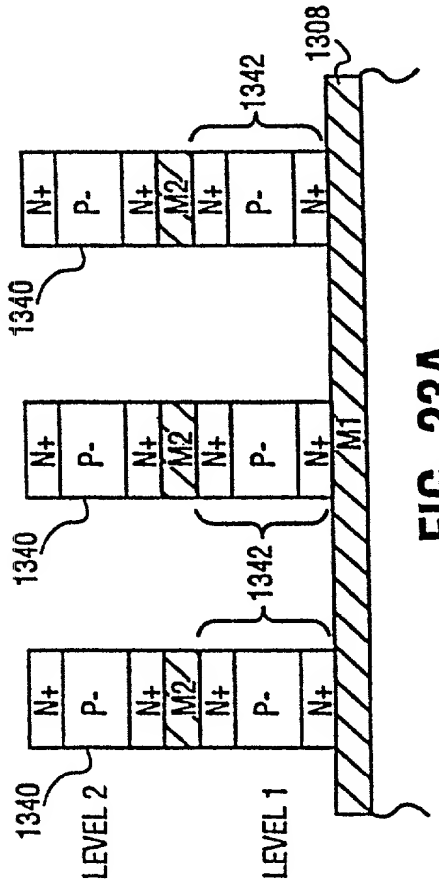


FIG. 23A

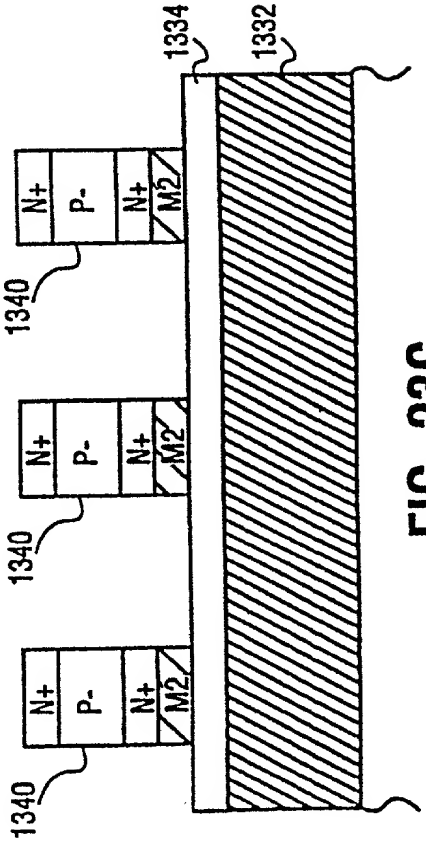
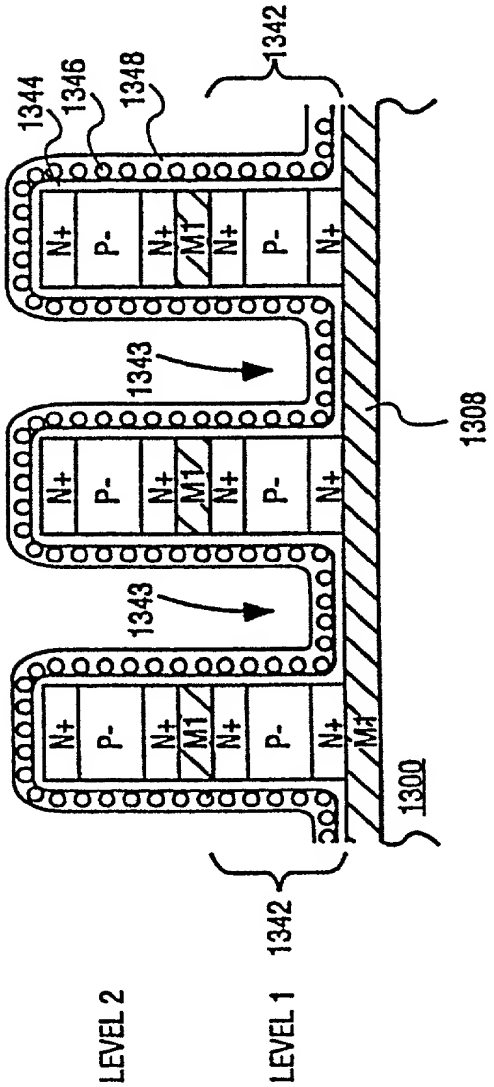


FIG. 23C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LEVEL 2
LEVEL 1

FIG. 24

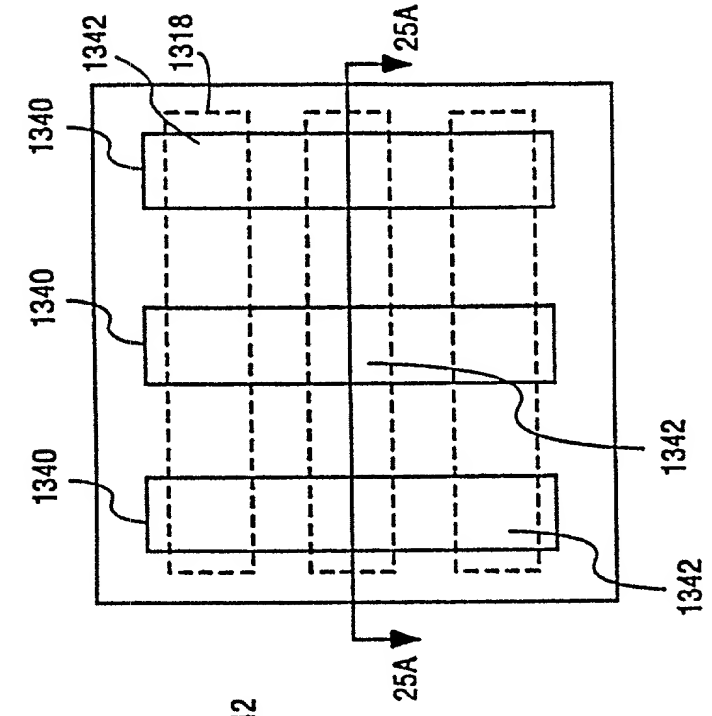


FIG. 25B

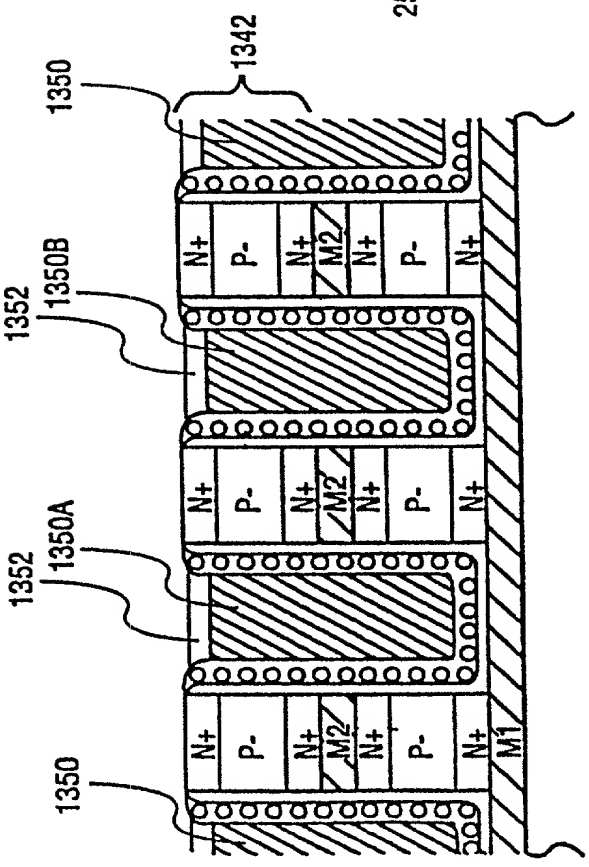


FIG. 25A

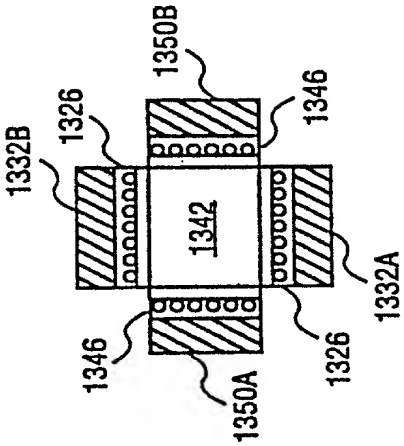


FIG. 26

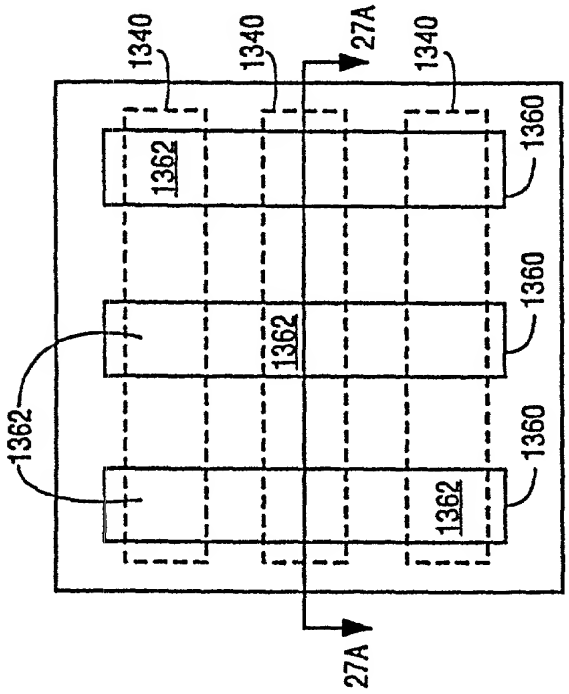


FIG. 27B

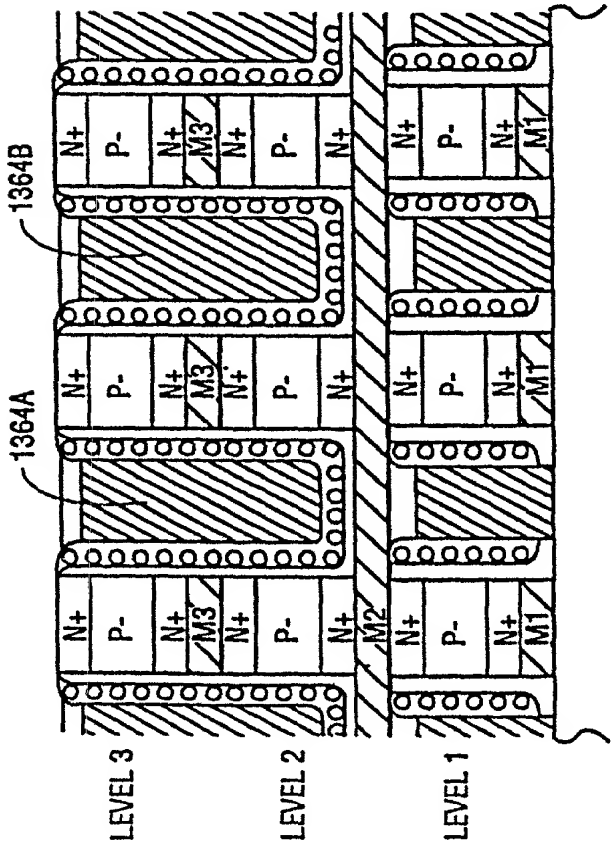


FIG. 27A

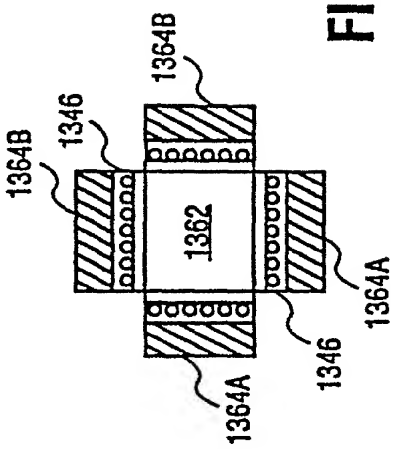


FIG. 28

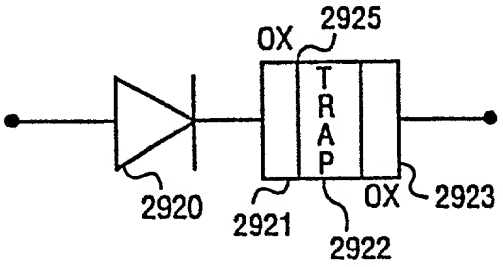


FIG. 29A

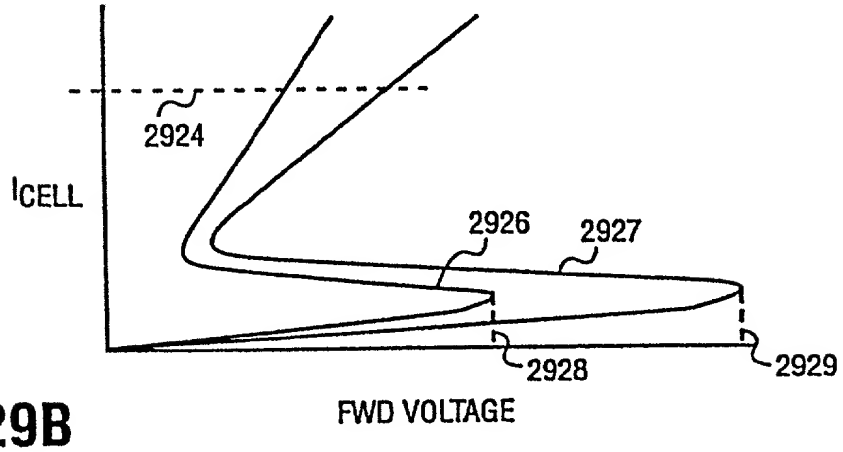


FIG. 29B

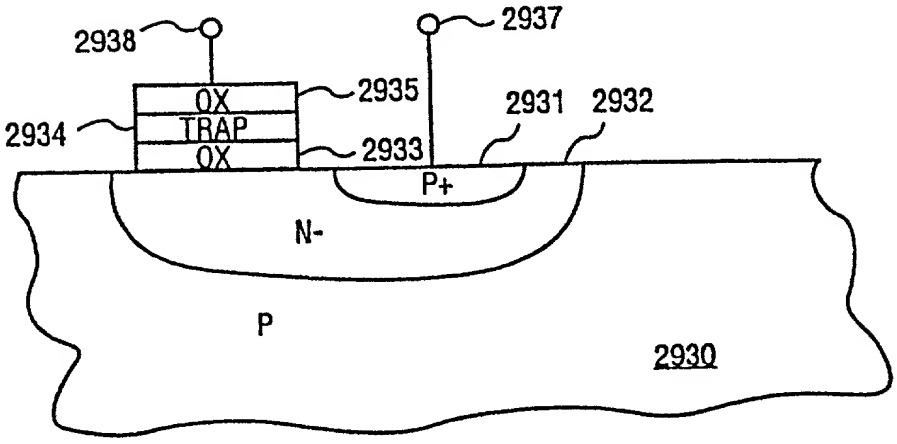

2938
2937
OX
TRAP
OX
2935
2933
2934
2931
2932
P+
N-
P
2930

FIG. 30

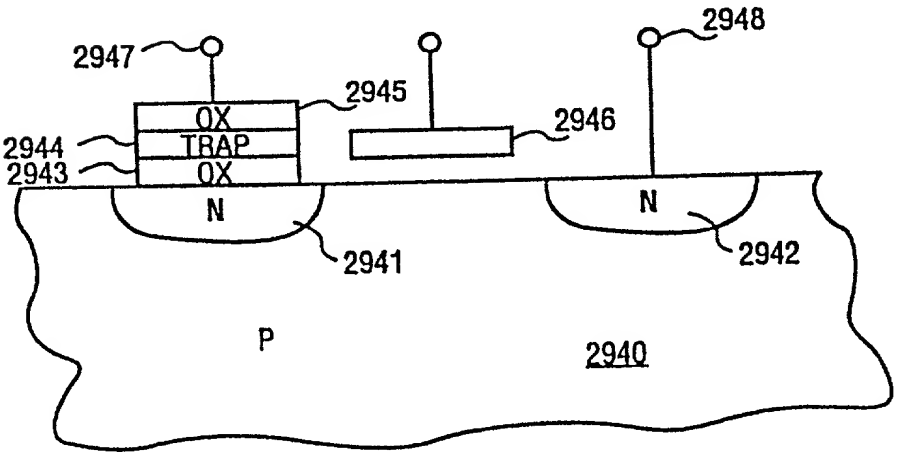

2947
2948
2945
2946
OX
TRAP
OX
2944
2943
N
N
2941
2942
P
2940

FIG. 31

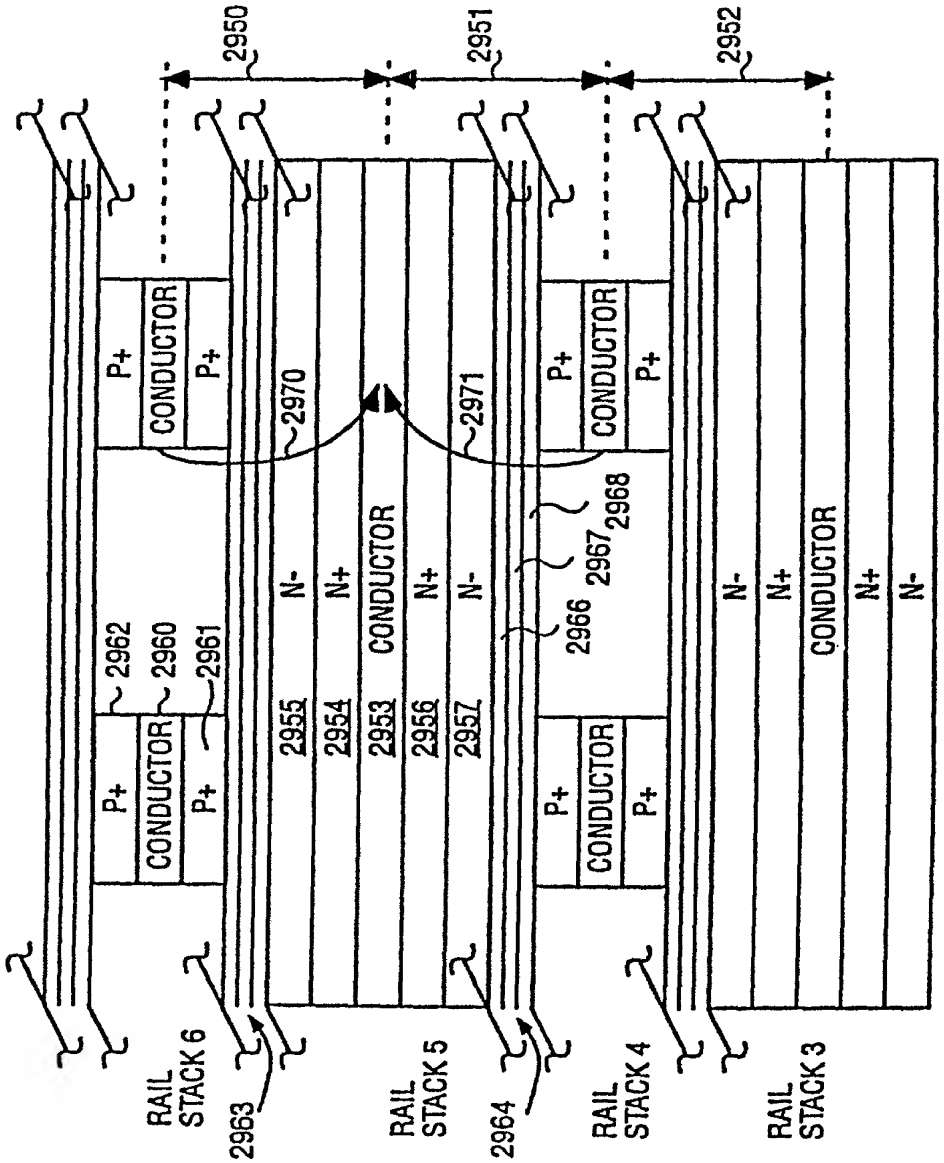

2950
2951
2952
P+
CONDUCTOR
P+
2962
2960
2961
2970
2971
2968
2967
2966
N-
N+
CONDUCTOR
2955
2954
2953
2956
2957
RAIL STACK 6
RAIL STACK 5
RAIL STACK 4
RAIL STACK 3
2963
2964

FIG. 32

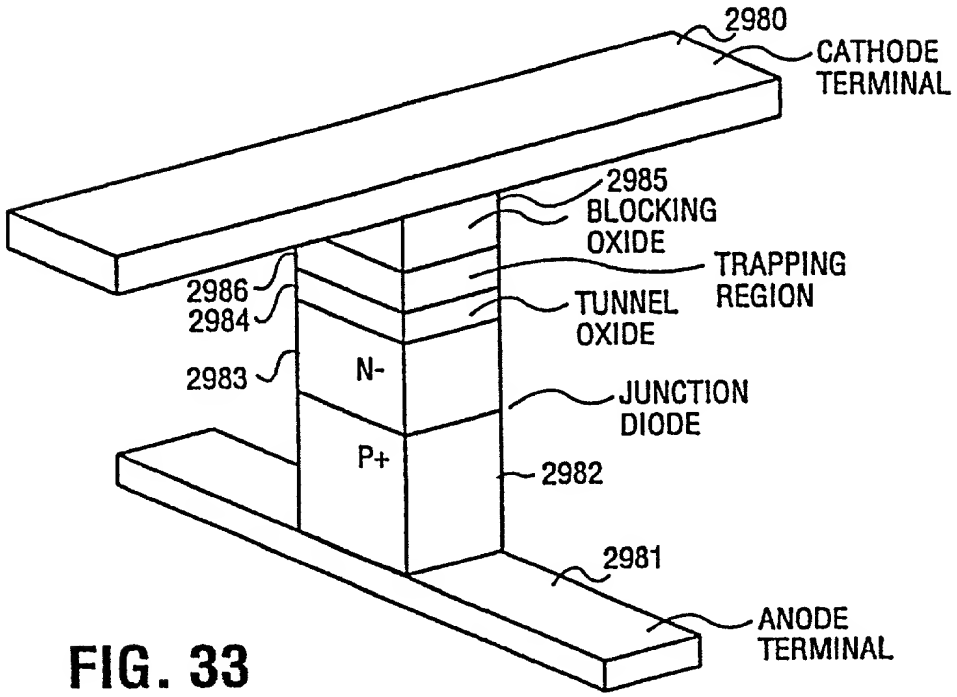

2980
CATHODE TERMINAL
2985
BLOCKING OXIDE
TRAPPING REGION
TUNNEL OXIDE
2986
2984
2983
N-
JUNCTION DIODE
P+
2982
2981
ANODE TERMINAL

FIG. 33

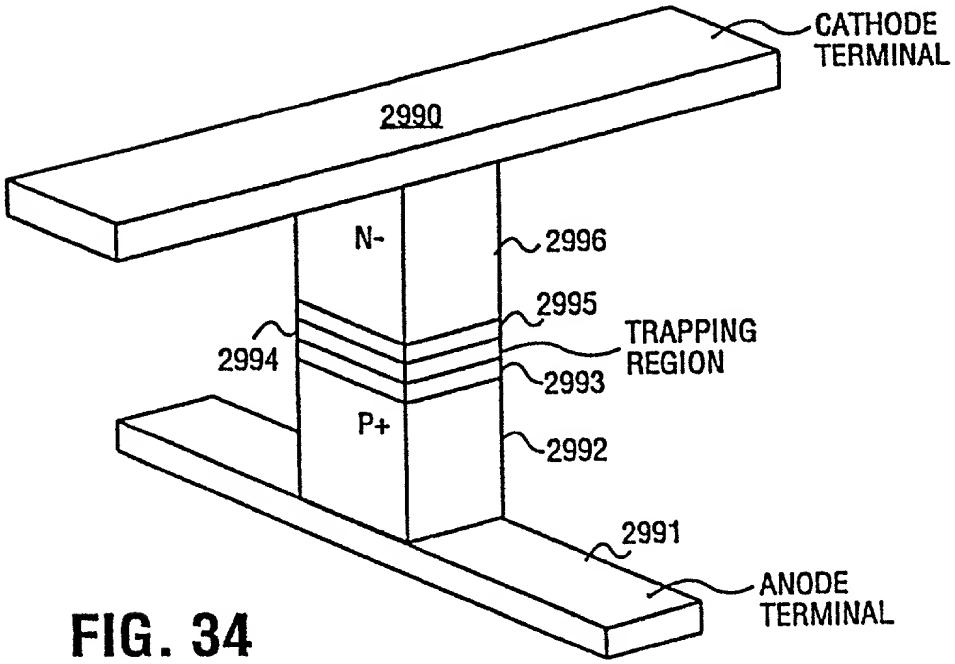

CATHODE TERMINAL
2990
N-
2996
2995
TRAPPING REGION
2994
2993
P+
2992
2991
ANODE TERMINAL

FIG. 34

FIG. 35

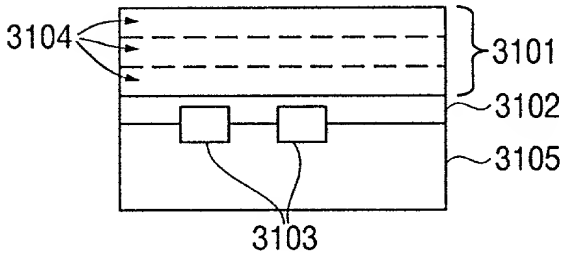


FIG. 36

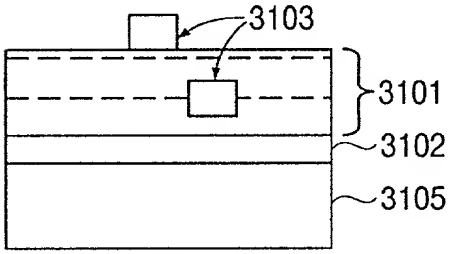


FIG. 37

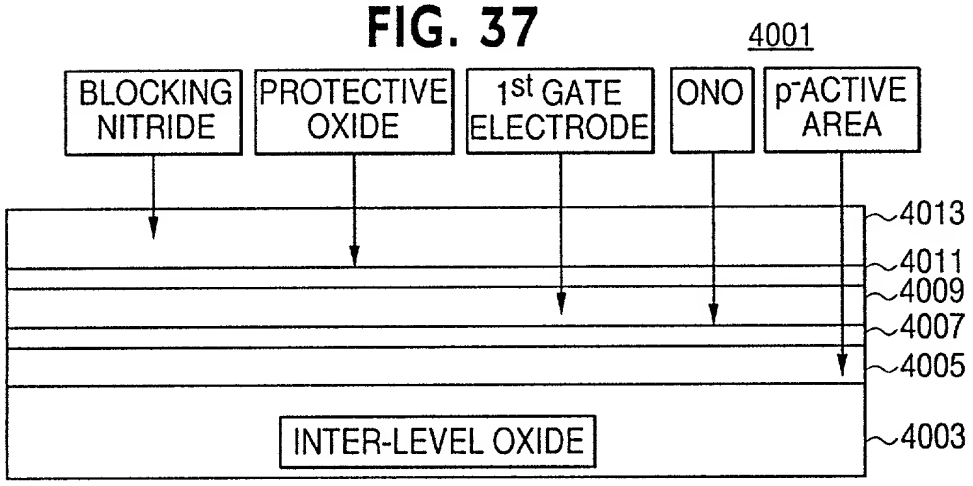

4001
BLOCKING NITRIDE
PROTECTIVE OXIDE
1st GATE ELECTRODE
ONO
p- ACTIVE AREA
4013
4011
4009
4007
4005
INTER-LEVEL OXIDE
4003

FIG. 38

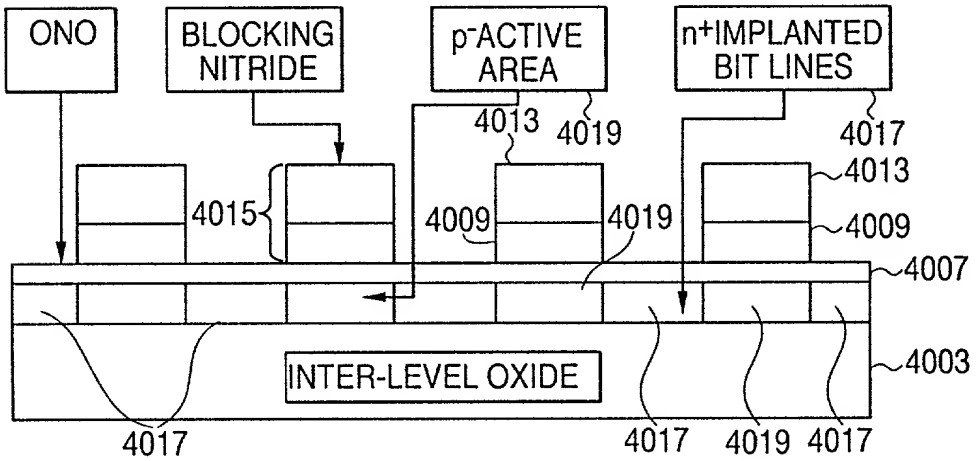

ONO
BLOCKING NITRIDE
p- ACTIVE AREA
n+ IMPLANTED BIT LINES
4013
4019
4017
4015
4009
4019
4013
4009
4007
INTER-LEVEL OXIDE
4003
4017
4017
4019
4017

FIG. 39

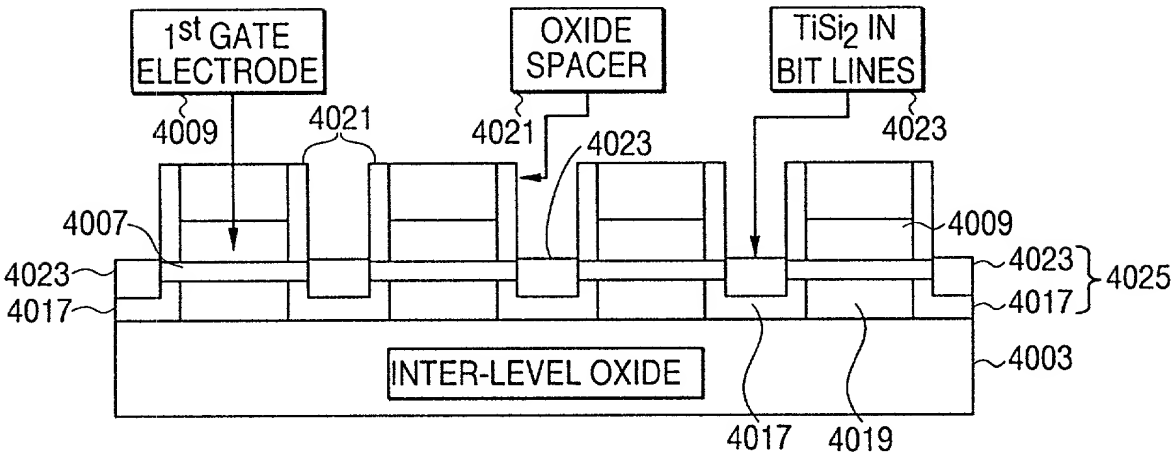

1st GATE ELECTRODE
OXIDE SPACER
TiSi2 IN BIT LINES
4009
4021
4021
4023
4023
4007
4009
4023
4025
4023
4017
4017
INTER-LEVEL OXIDE
4003
4017
4019

FIG. 40

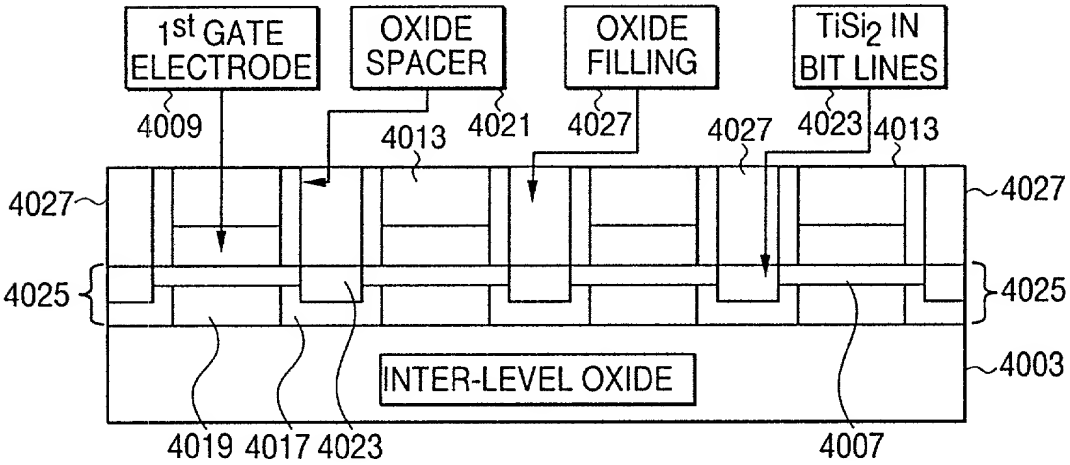

1st GATE ELECTRODE
OXIDE SPACER
OXIDE FILLING
TiSi2 IN BIT LINES
4009
4013
4021
4027
4027
4023
4013
4027
4027
4025
4025
INTER-LEVEL OXIDE
4003
4019
4017
4023
4007

FIG. 41

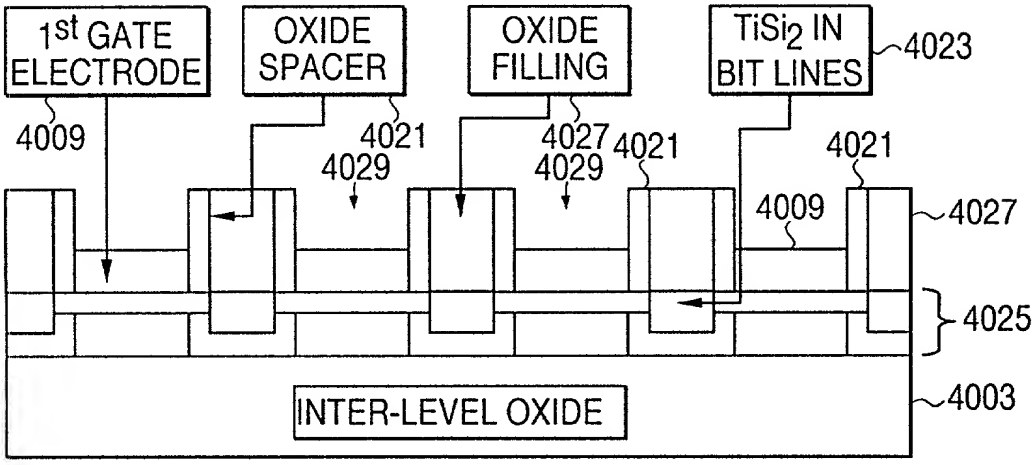

1st GATE ELECTRODE
OXIDE SPACER
OXIDE FILLING
TiSi2 IN BIT LINES
4023
4009
4021
4029
4027
4029
4021
4021
4009
4027
4025
INTER-LEVEL OXIDE
4003

FIG. 42

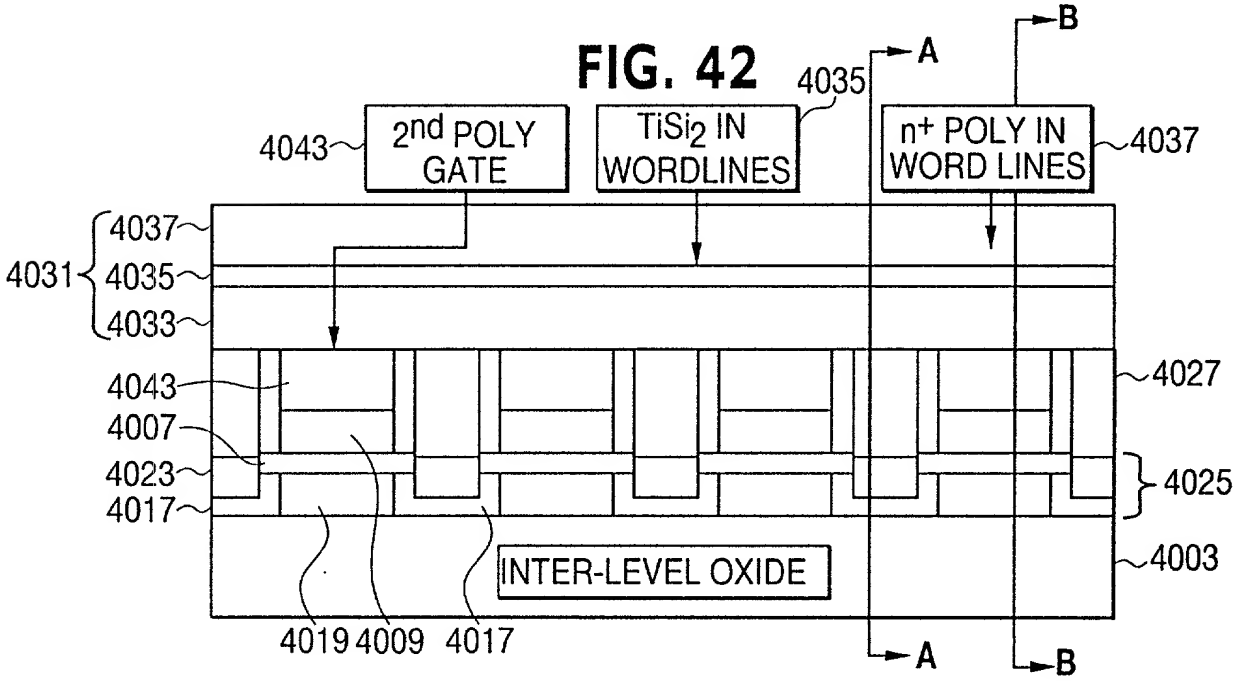

B
A
4035
4043
2nd POLY GATE
TiSi2 IN WORDLINES
n+ POLY IN WORD LINES
4037
4037
4031
4035
4033
4043
4007
4023
4017
4027
4025
INTER-LEVEL OXIDE
4003
4019
4009
4017
A
B

FIG. 43

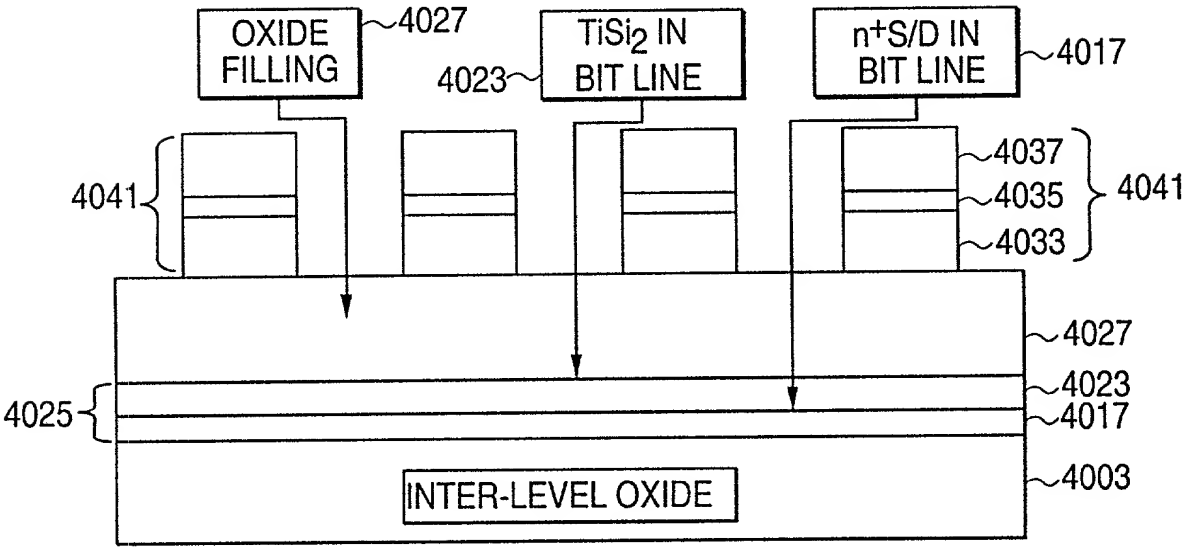

OXIDE FILLING
4027
TiSi2 IN BIT LINE
4023
n+S/D IN BIT LINE
4017
4041
4037
4035
4033
4041
4027
4023
4017
4025
INTER-LEVEL OXIDE
4003

FIG. 44

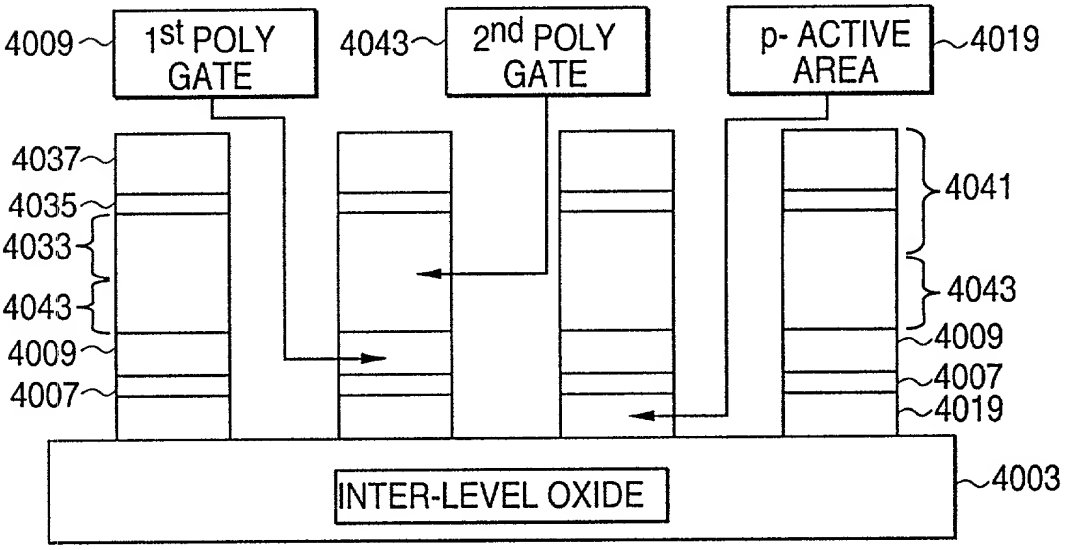

4009
1st POLY GATE
4043
2nd POLY GATE
p- ACTIVE AREA
4019
4037
4035
4033
4043
4009
4007
4041
4043
4009
4007
4019
INTER-LEVEL OXIDE
4003

FIG. 45

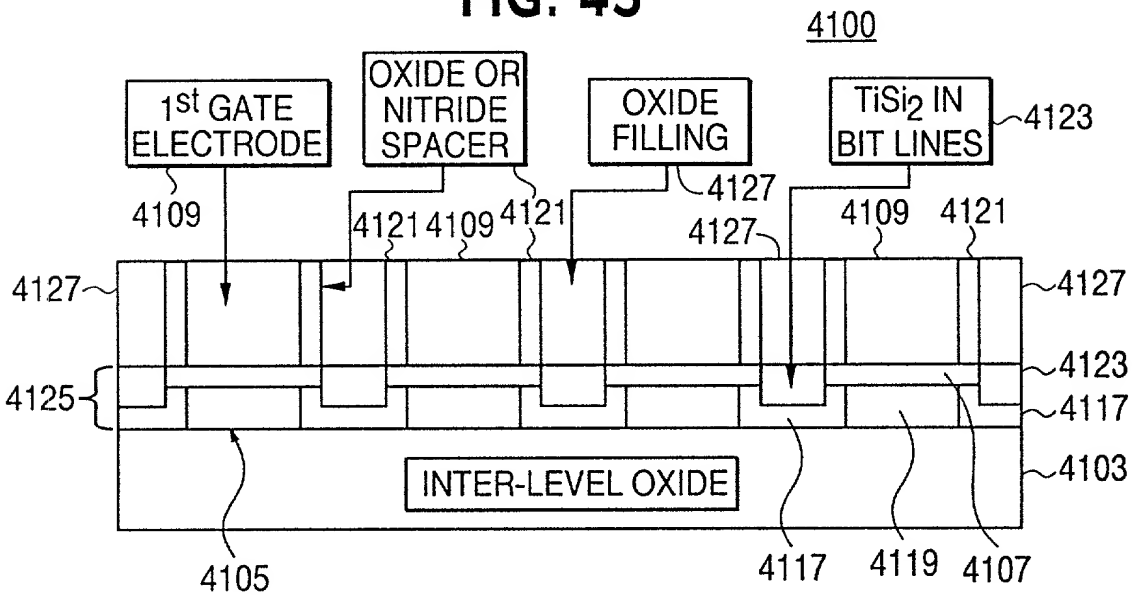


FIG. 46

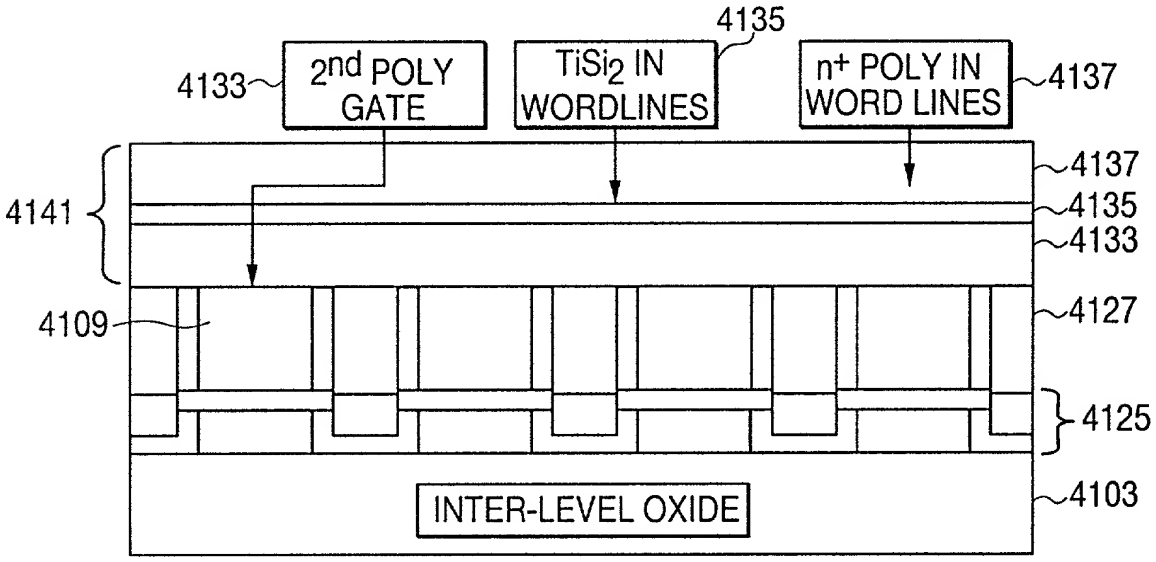
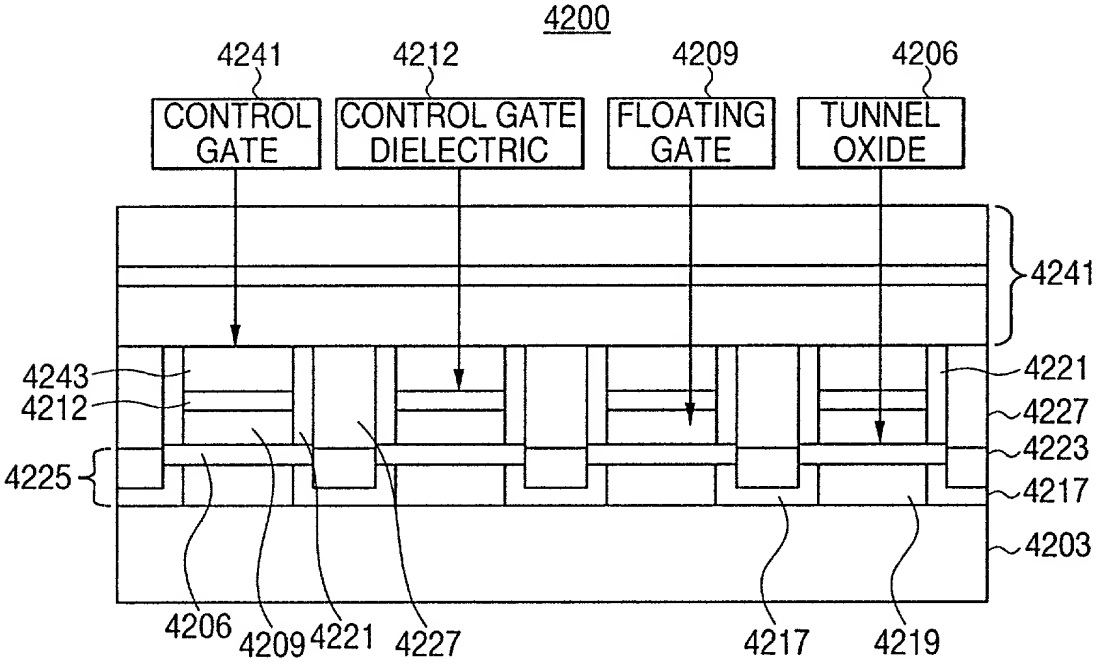


FIG. 47


4200
4241
4212
4209
4206
CONTROL GATE
CONTROL GATE DIELECTRIC
FLOATING GATE
TUNNEL OXIDE
4241
4243
4212
4225
4221
4227
4223
4217
4203
4206
4209
4221
4227
4217
4219

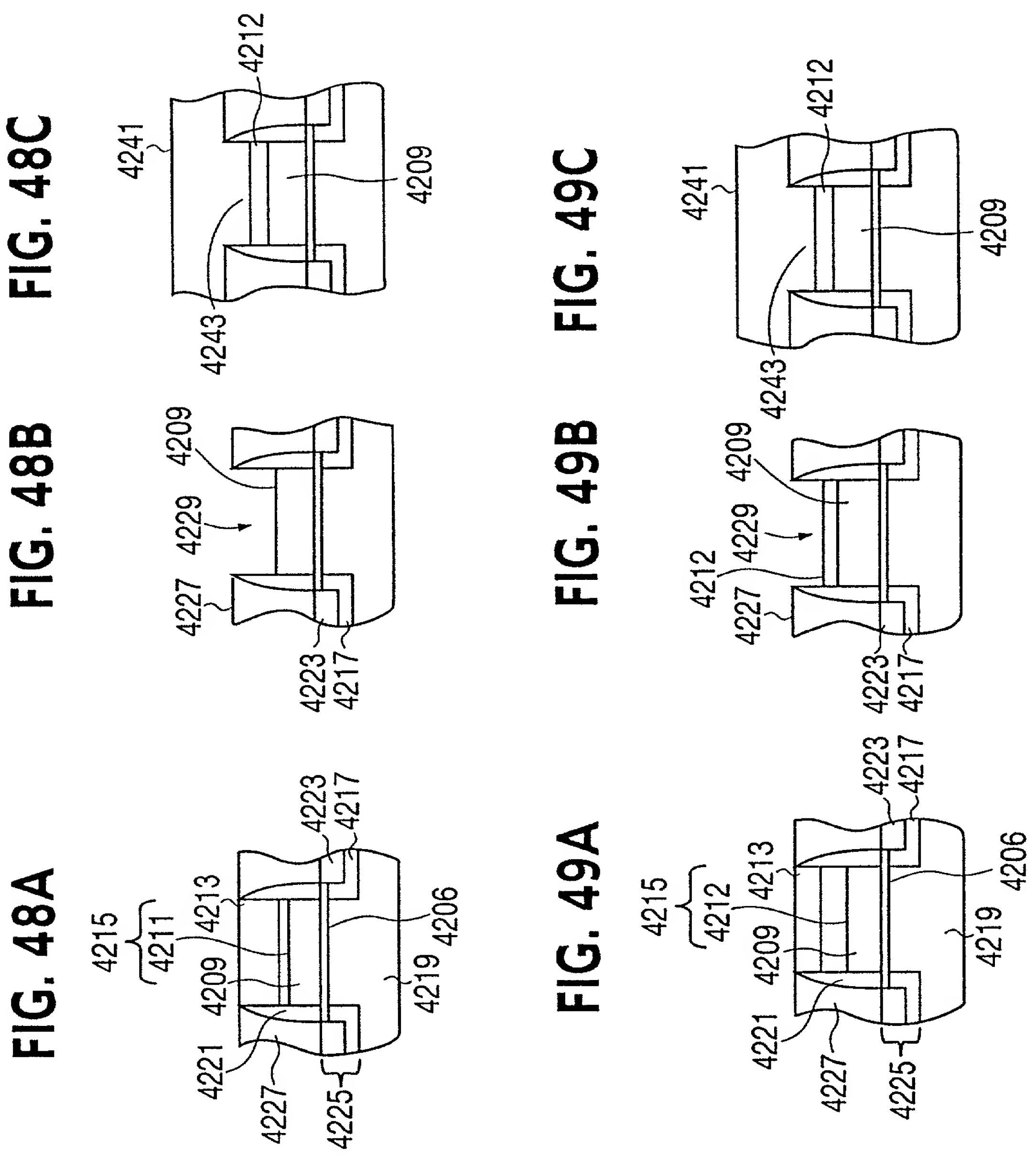


FIG. 48A FIG. 48B FIG. 48C

FIG. 49A FIG. 49B FIG. 49C

FIG. 50

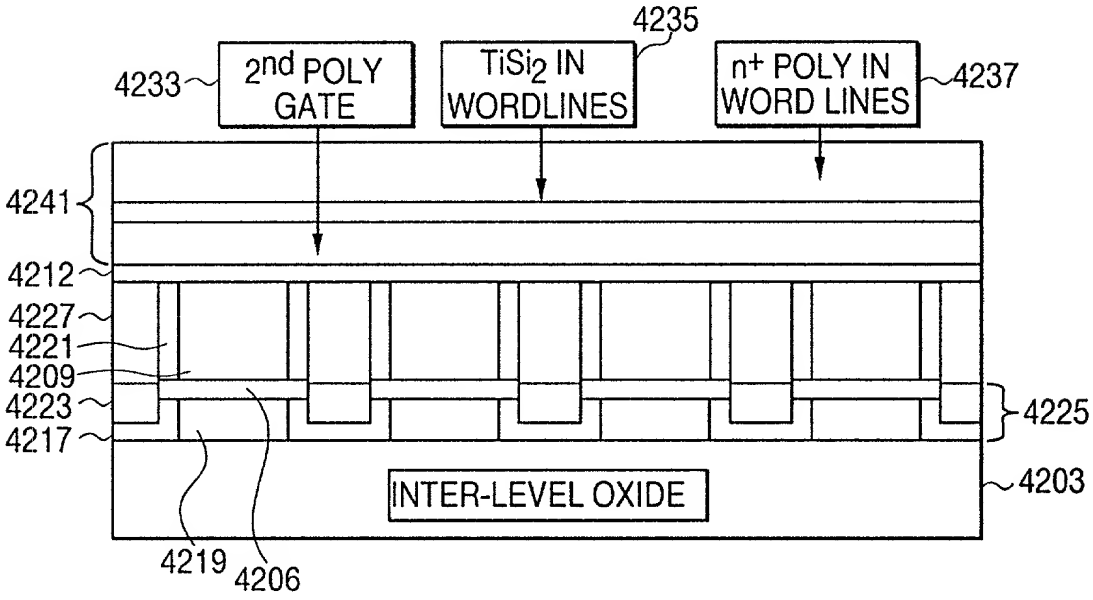

4235
4233
2nd POLY GATE
TiSi2 IN WORDLINES
n+ POLY IN WORD LINES
4237
4241
4212
4227
4221
4209
4223
4217
4225
INTER-LEVEL OXIDE
4203
4219
4206

FIG. 51

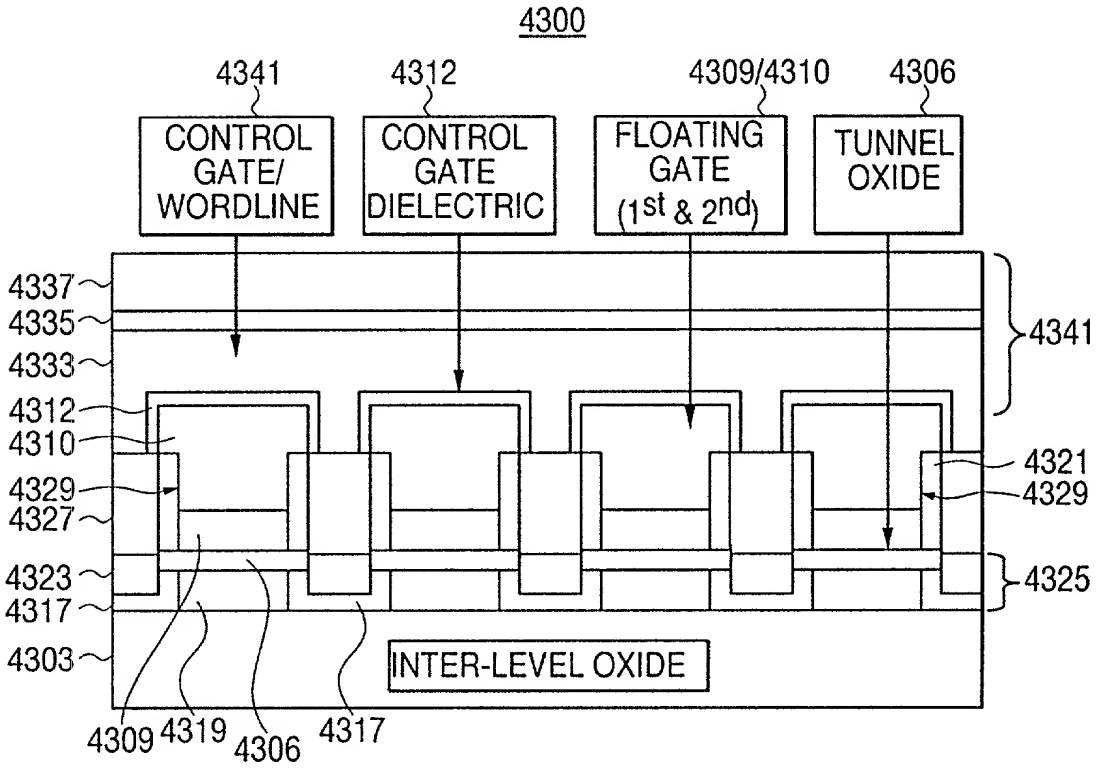

4300
4341
4312
4309/4310
4306
CONTROL GATE/ WORDLINE
CONTROL GATE DIELECTRIC
FLOATING GATE (1st & 2nd)
TUNNEL OXIDE
4337
4335
4333
4312
4310
4329
4327
4323
4317
4303
4341
4321
4329
4325
INTER-LEVEL OXIDE
4309
4319
4306
4317

FIG. 52

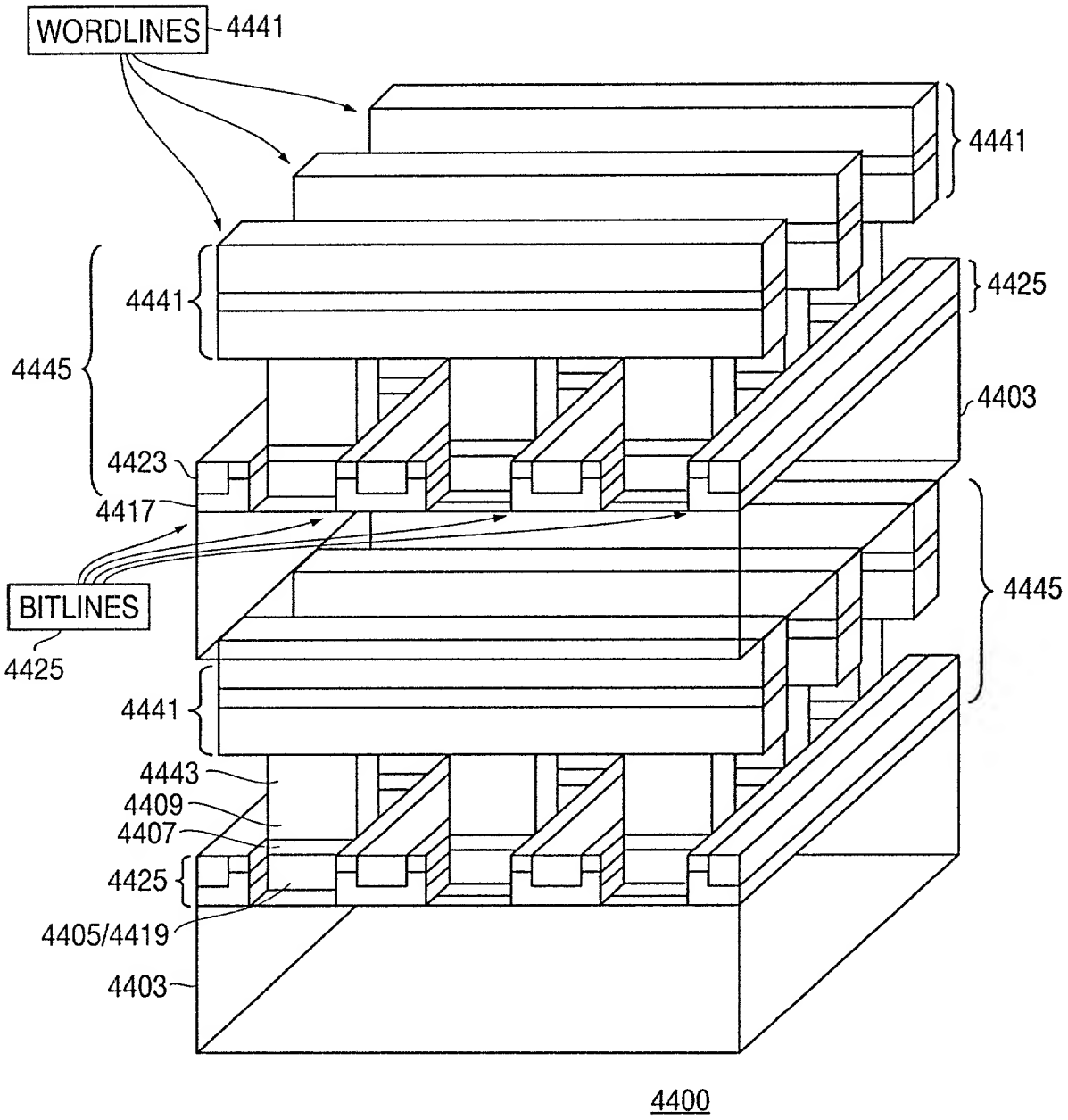

WORDLINES
4441
4441
4441
4425
4445
4403
4423
4417
BITLINES
4425
4445
4441
4443
4409
4407
4425
4405/4419
4403
4400

FIG. 53

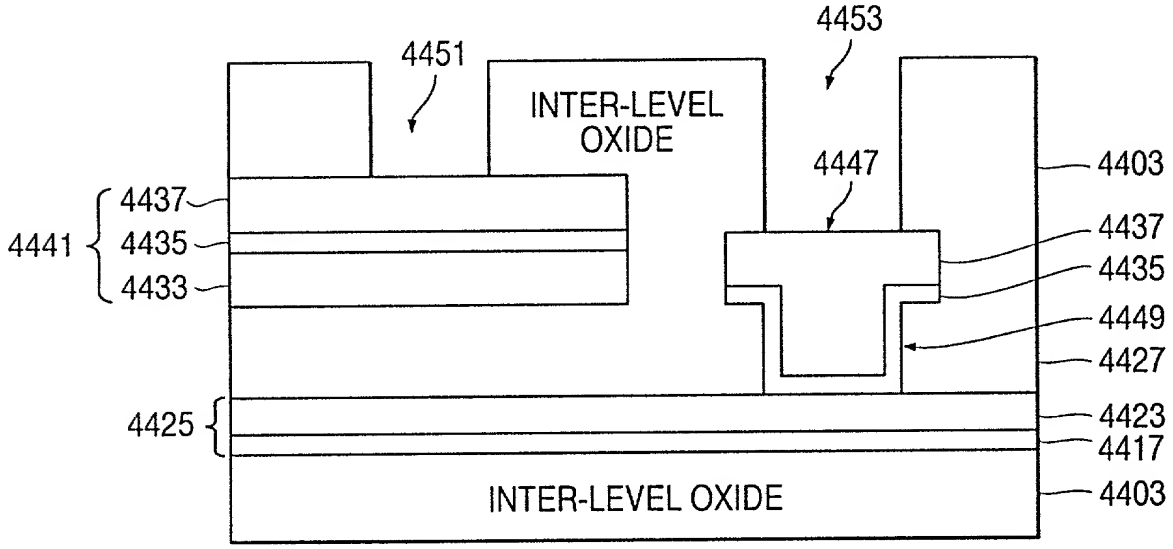


FIG. 54

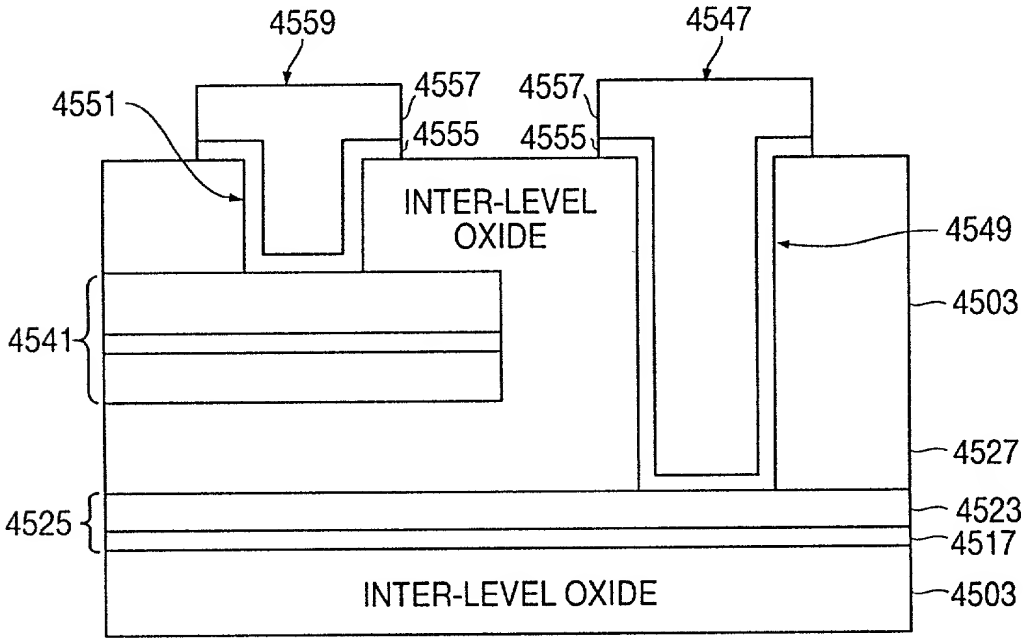


FIG. 55

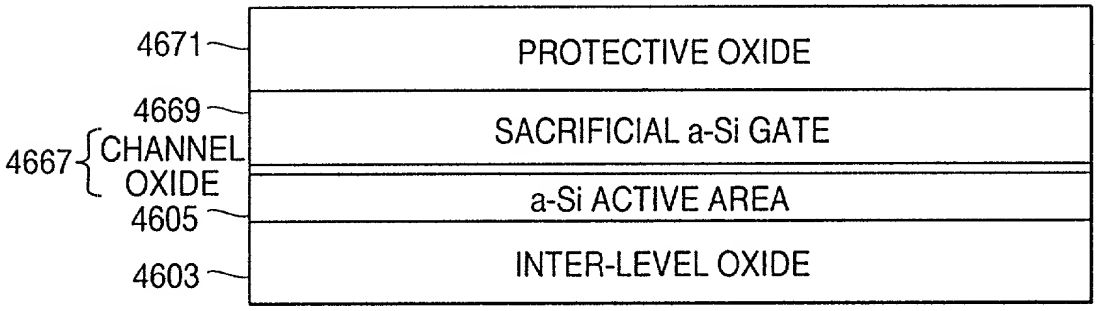


FIG. 56

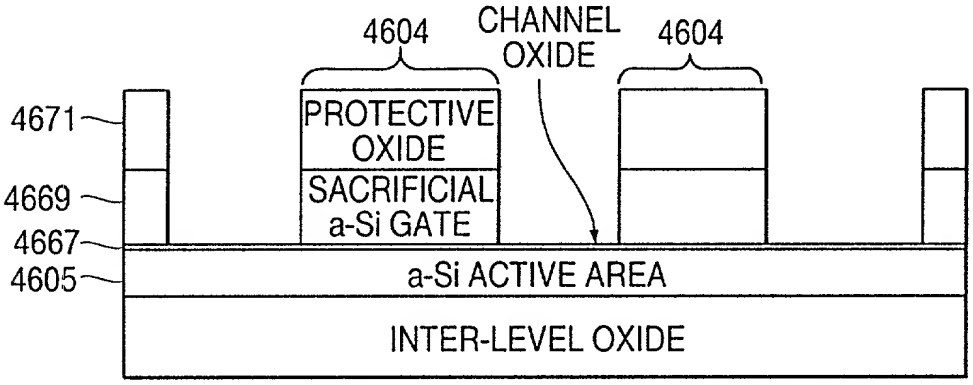


FIG. 57

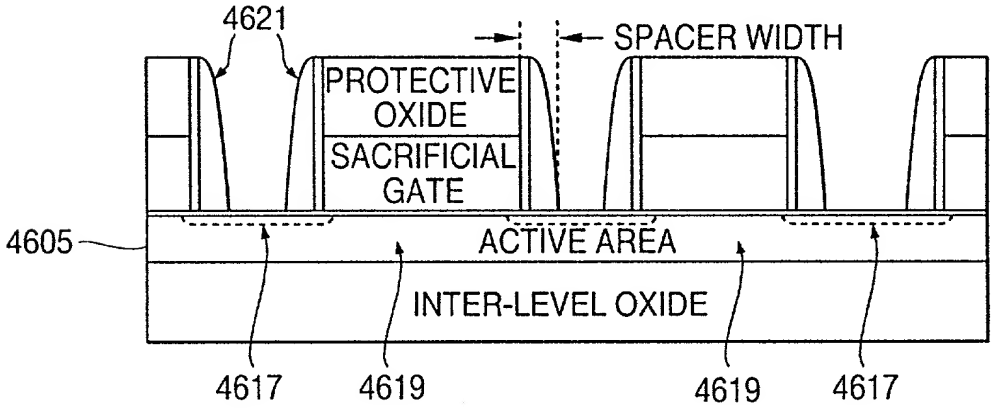


FIG. 58

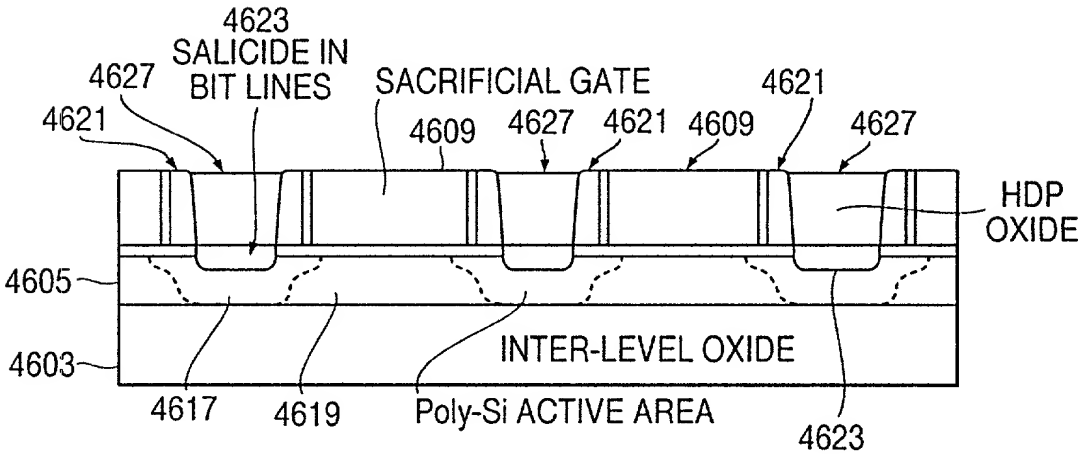

4623
SALICIDE IN
BIT LINES
4627
4621
SACRIFICIAL GATE
4609
4627
4621
4609
4621
4627
HDP
OXIDE
4605
4603
INTER-LEVEL OXIDE
4617
4619
Poly-Si ACTIVE AREA
4623

FIG. 59

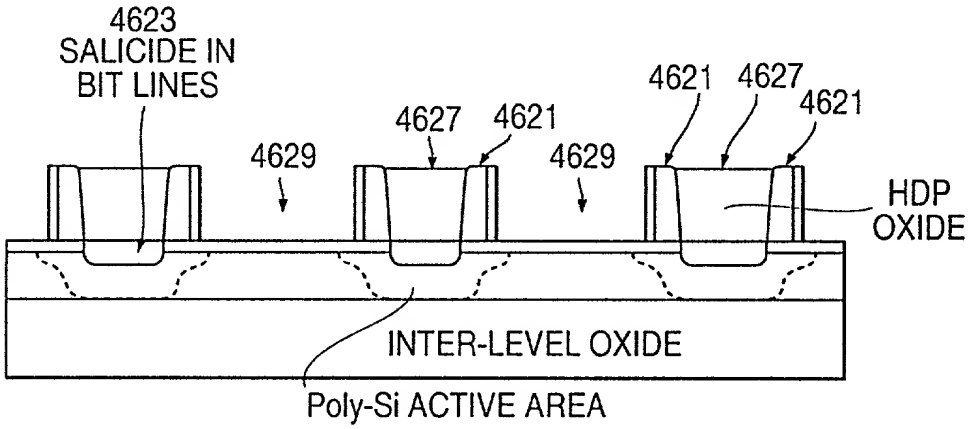

4623
SALICIDE IN
BIT LINES
4621
4627
4621
4627
4621
4629
4629
HDP
OXIDE
INTER-LEVEL OXIDE
Poly-Si ACTIVE AREA

FIG. 60

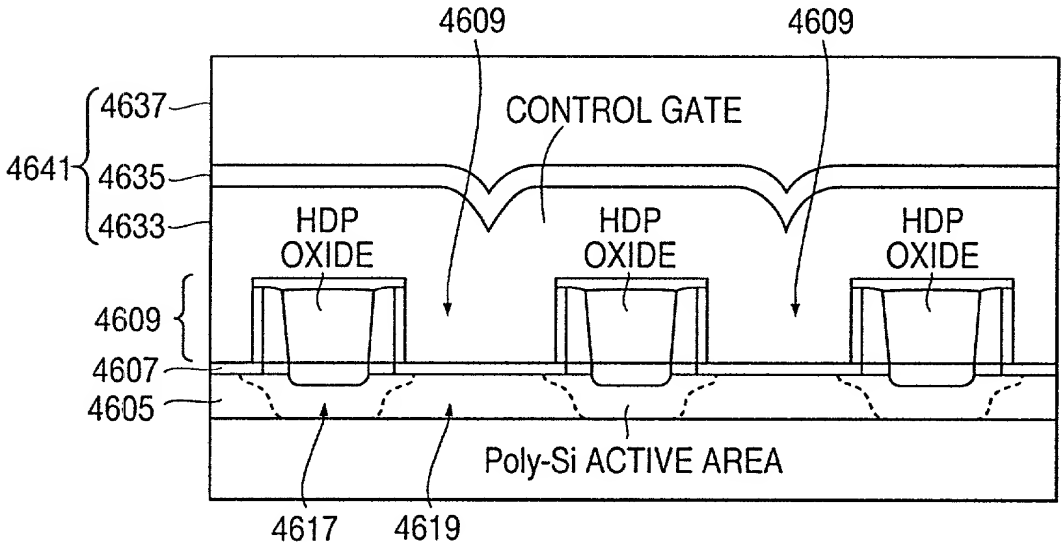

4609
4609
4637
CONTROL GATE
4641
4635
4633
HDP OXIDE
HDP OXIDE
HDP OXIDE
4609
4607
4605
Poly-Si ACTIVE AREA
4617
4619

FIG. 61

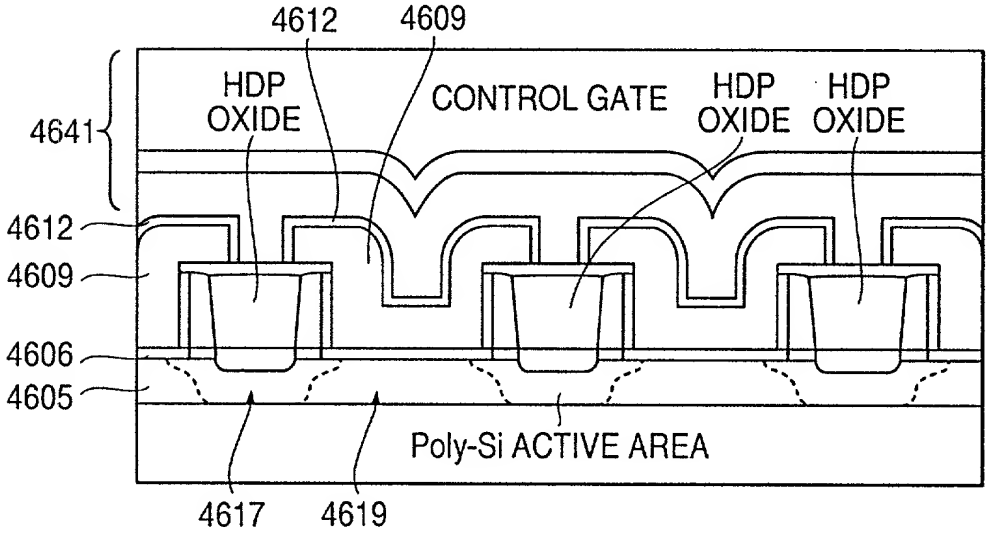

4612
4609
HDP OXIDE
CONTROL GATE
HDP OXIDE
HDP OXIDE
4641
4612
4609
4606
4605
Poly-Si ACTIVE AREA
4617
4619

FIG. 62

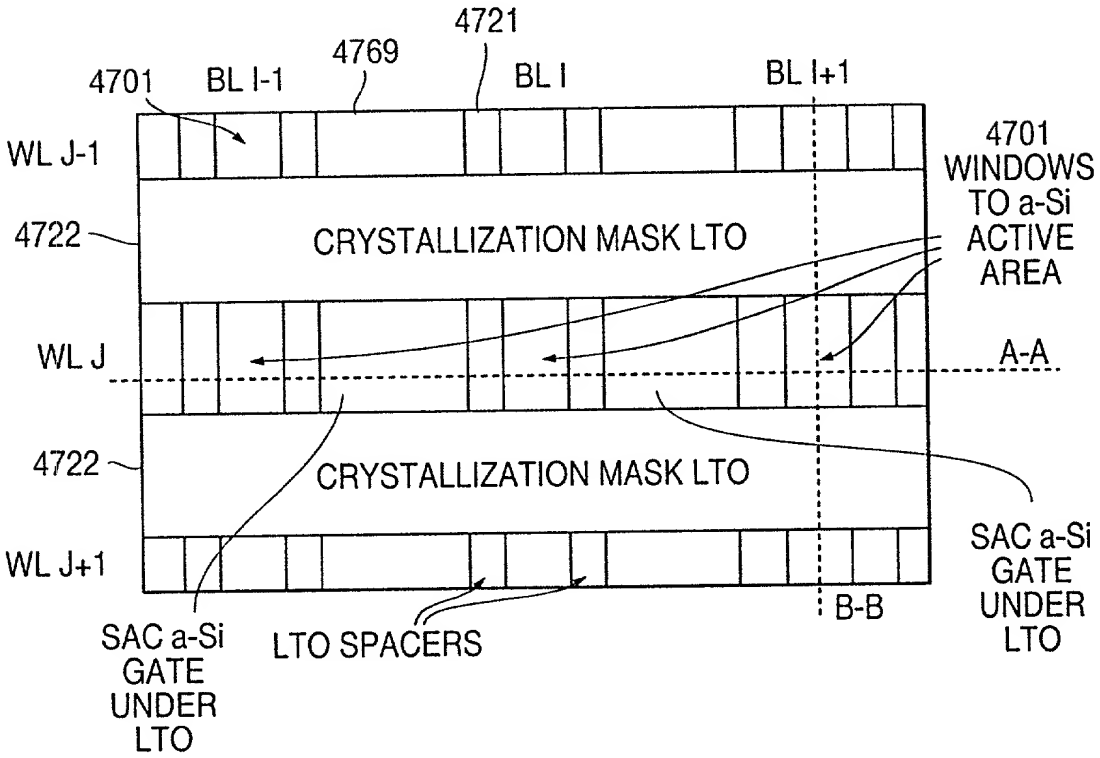

4721
4769
4701
BL I-1
BL I
BL I+1
WL J-1
4701 WINDOWS TO a-Si ACTIVE AREA
4722
CRYSTALLIZATION MASK LTO
WL J
A-A
4722
CRYSTALLIZATION MASK LTO
WL J+1
SAC a-Si GATE UNDER LTO
B-B
SAC a-Si GATE UNDER LTO
LTO SPACERS

FIG. 63

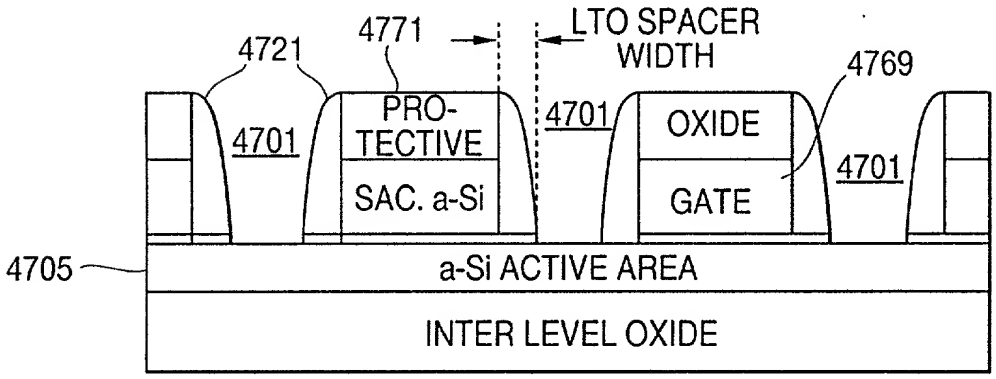

4721
4771
LTO SPACER WIDTH
4769
4701
PRO-TECTIVE
4701
OXIDE
4701
SAC. a-Si
GATE
4705
a-Si ACTIVE AREA
INTER LEVEL OXIDE

FIG. 64

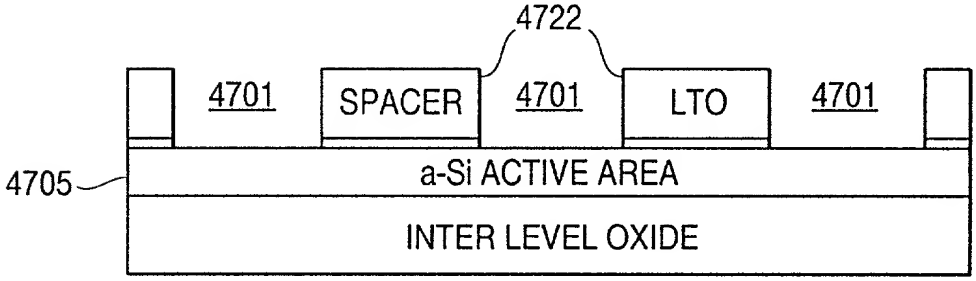

4722
4701
SPACER
4701
LTO
4701
4705
a-Si ACTIVE AREA
INTER LEVEL OXIDE

FIG. 65

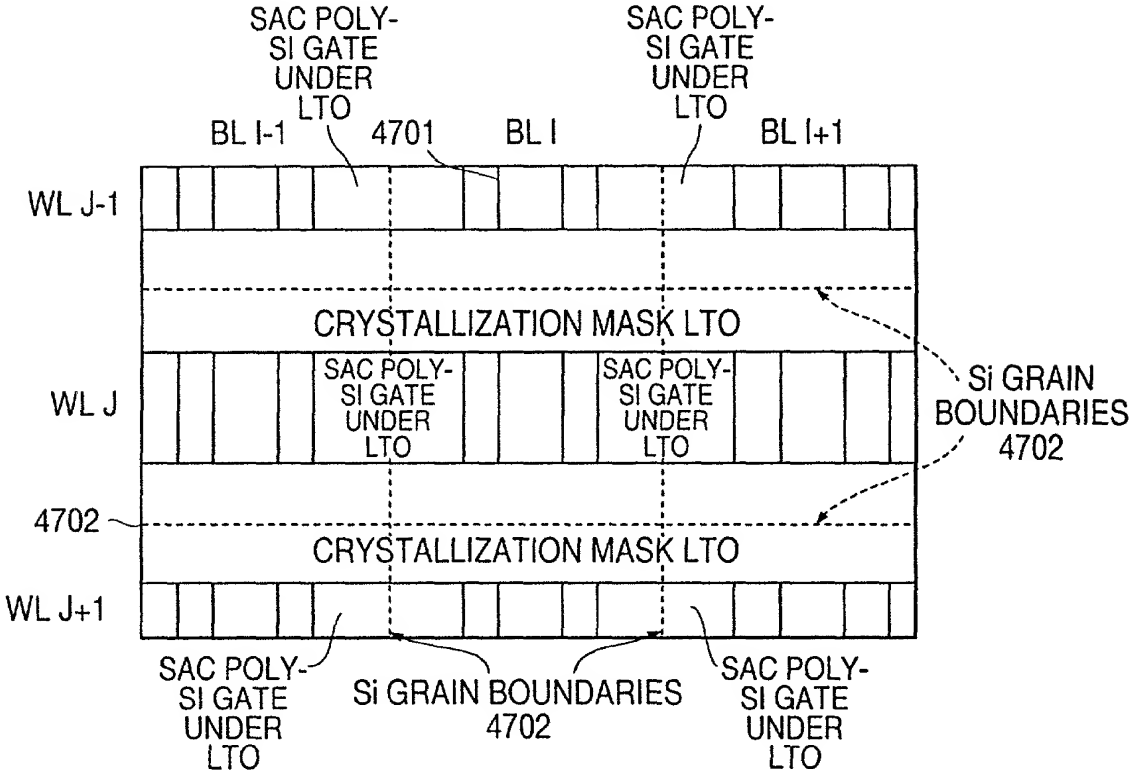
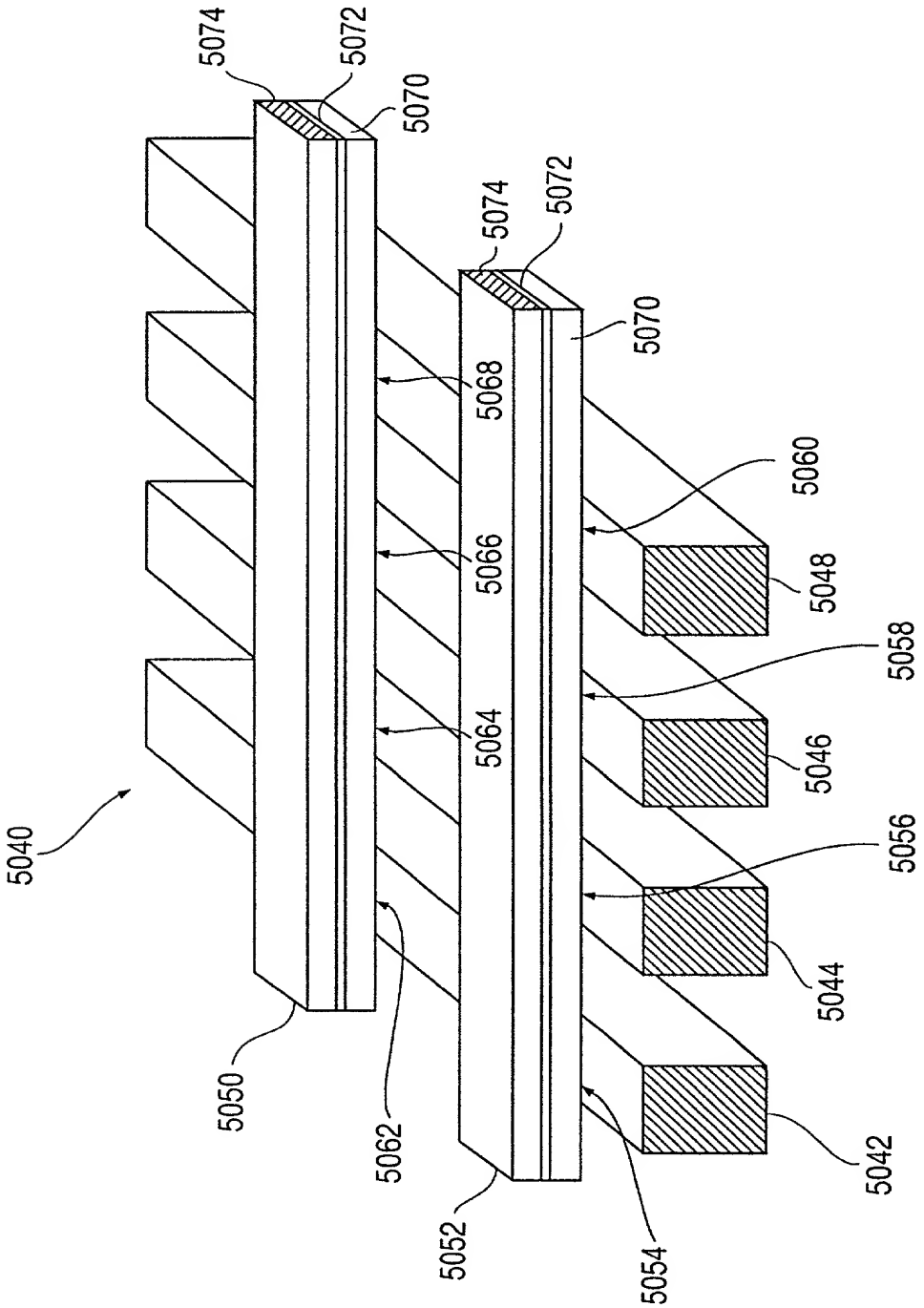

SAC POLY-SI GATE UNDER LTO
SAC POLY-SI GATE UNDER LTO
BL I-1
4701
BL I
BL I+1
WL J-1
CRYSTALLIZATION MASK LTO
WL J
SAC POLY-SI GATE UNDER LTO
SAC POLY-SI GATE UNDER LTO
Si GRAIN BOUNDARIES 4702
4702
CRYSTALLIZATION MASK LTO
WL J+1
SAC POLY-SI GATE UNDER LTO
Si GRAIN BOUNDARIES 4702
SAC POLY-SI GATE UNDER LTO

FIG. 66


5074
5072
5070
5074
5072
5070
5068
5060
5066
5048
5058
5064
5046
5056
5040
5044
5050
5062
5042
5052
5054

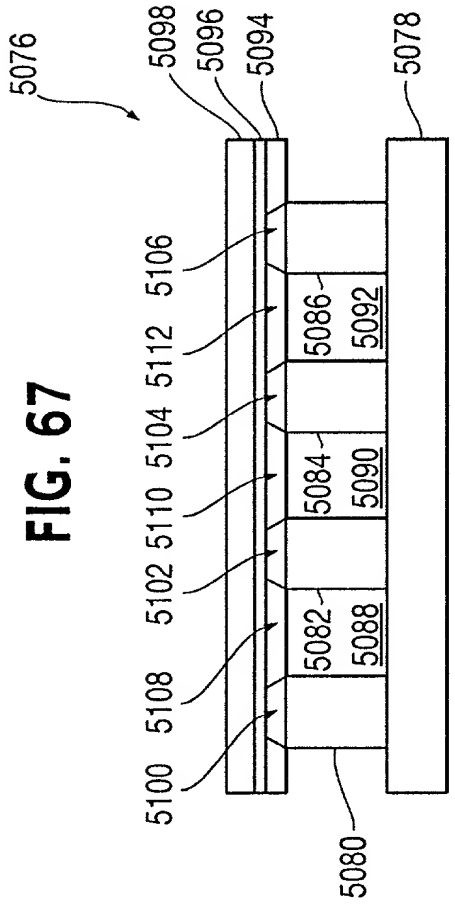


FIG. 67

FIG. 68

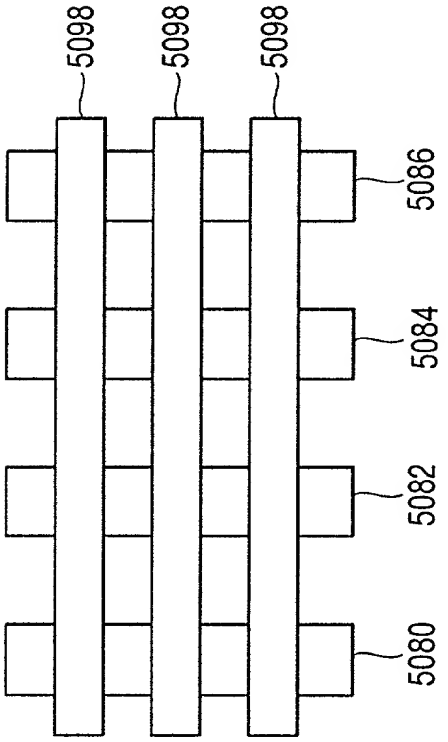


FIG. 69

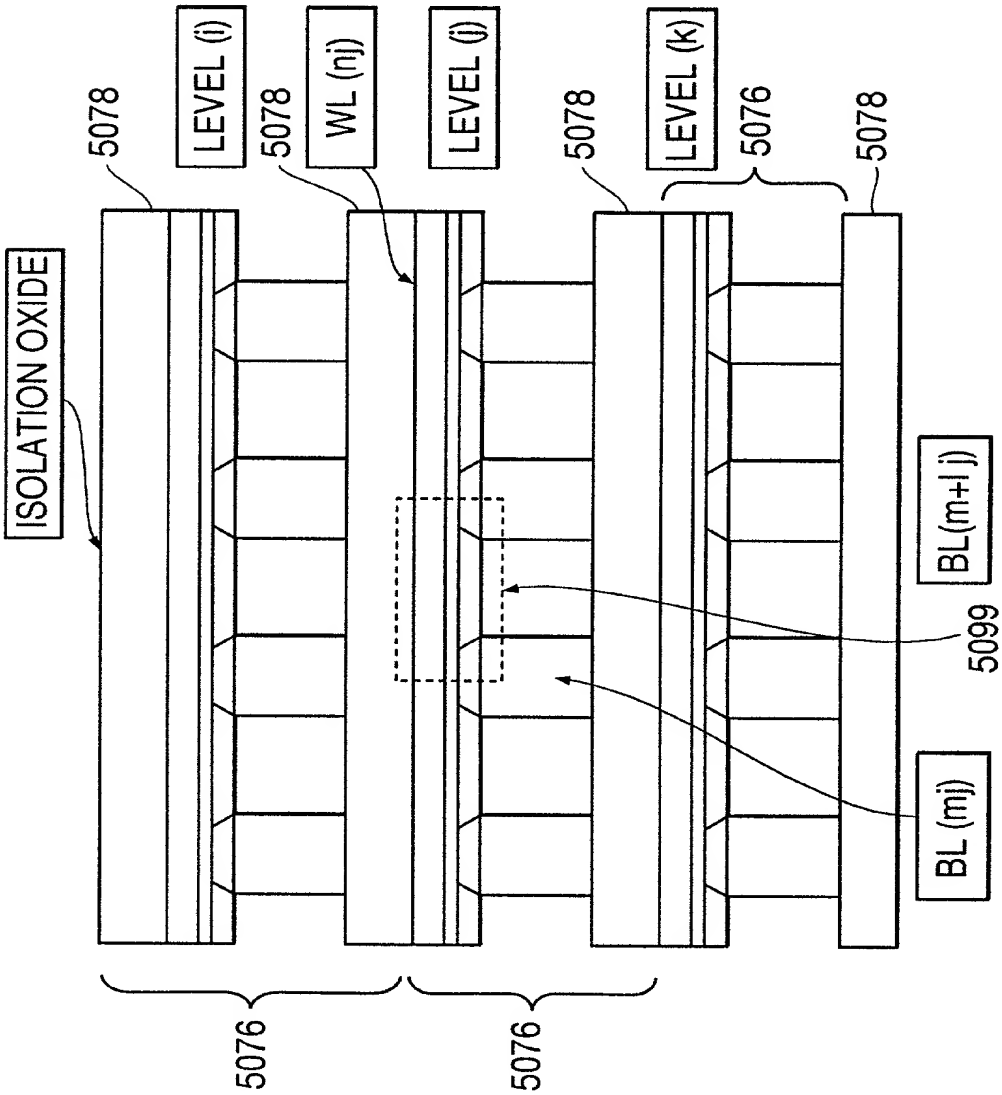


FIG. 70

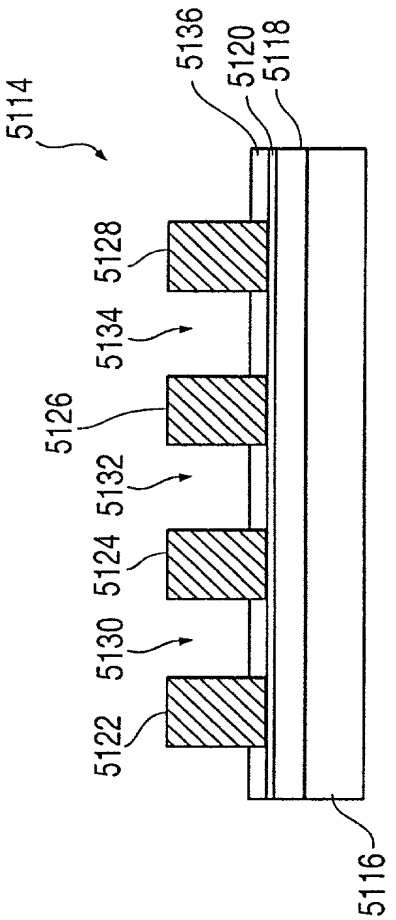
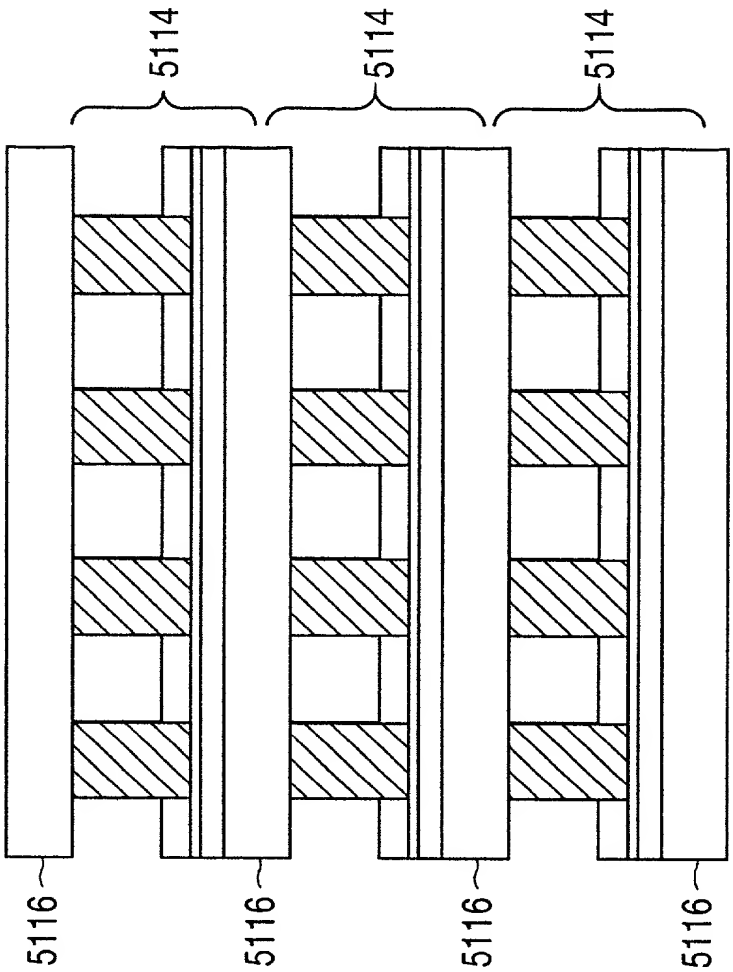


FIG. 71



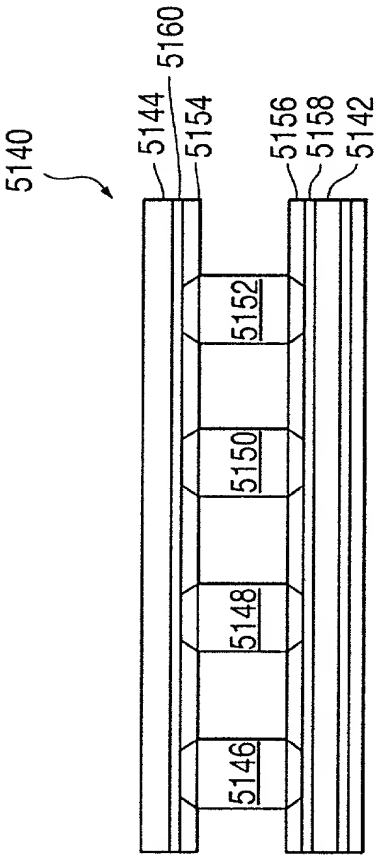


FIG. 72

FIG. 73

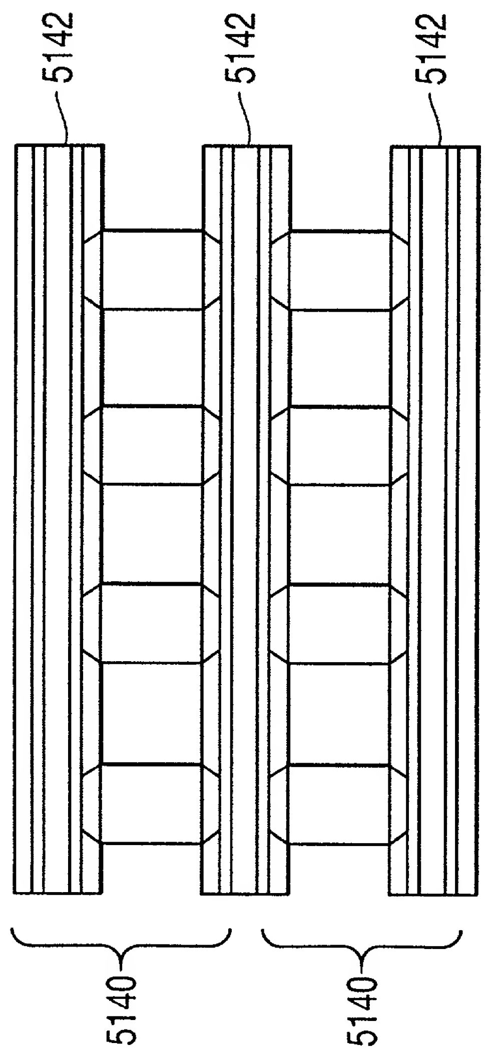


FIG. 74

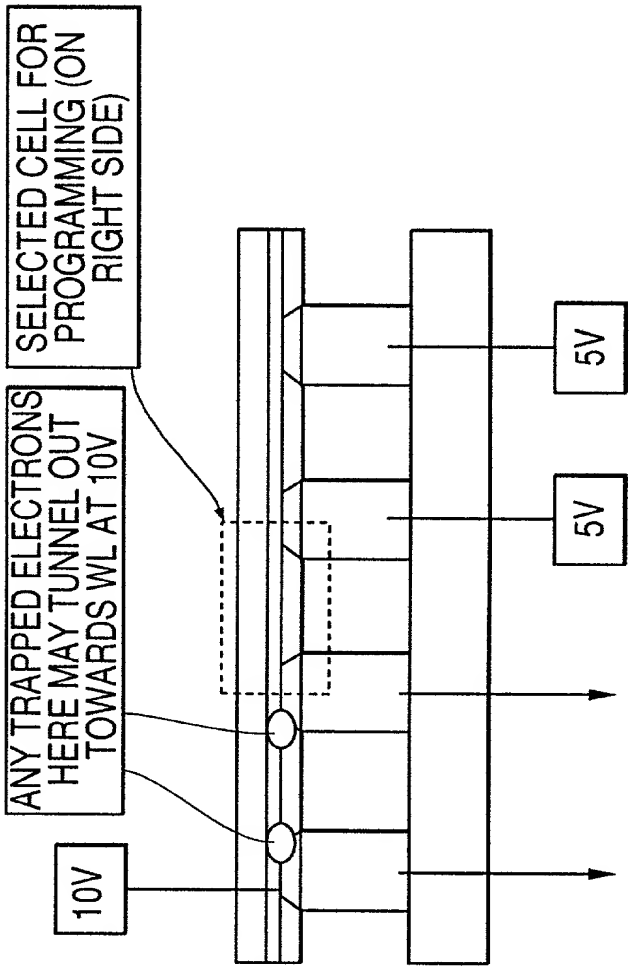

SELECTED CELL FOR PROGRAMMING (ON RIGHT SIDE)
ANY TRAPPED ELECTRONS HERE MAY TUNNEL OUT TOWARDS WL AT 10V
10V
5V
5V

FIG. 75

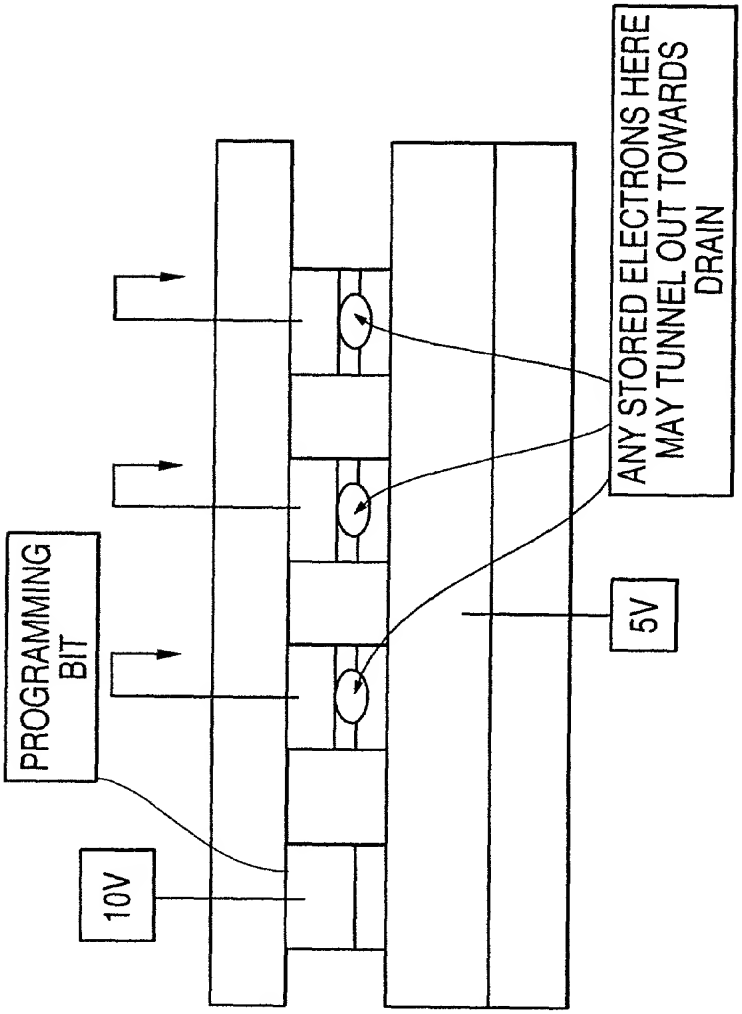

ANY STORED ELECTRONS HERE MAY TUNNEL OUT TOWARDS DRAIN
PROGRAMMING BIT
5V
10V

FIG. 76

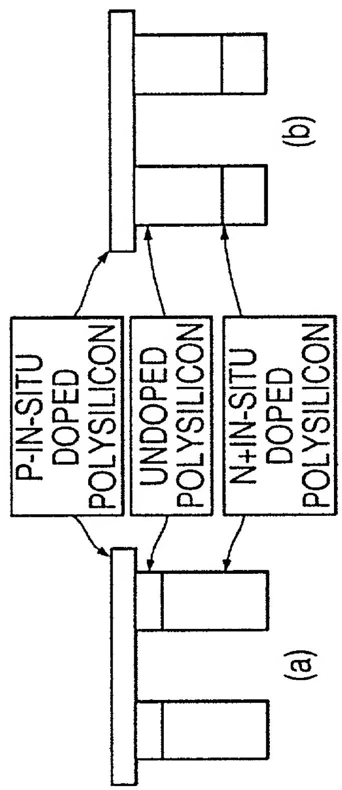

P-IN-SITU DOPED POLYSILICON
UNDOPED POLYSILICON
N+IN-SITU DOPED POLYSILICON
(a)
(b)

FIG. 77

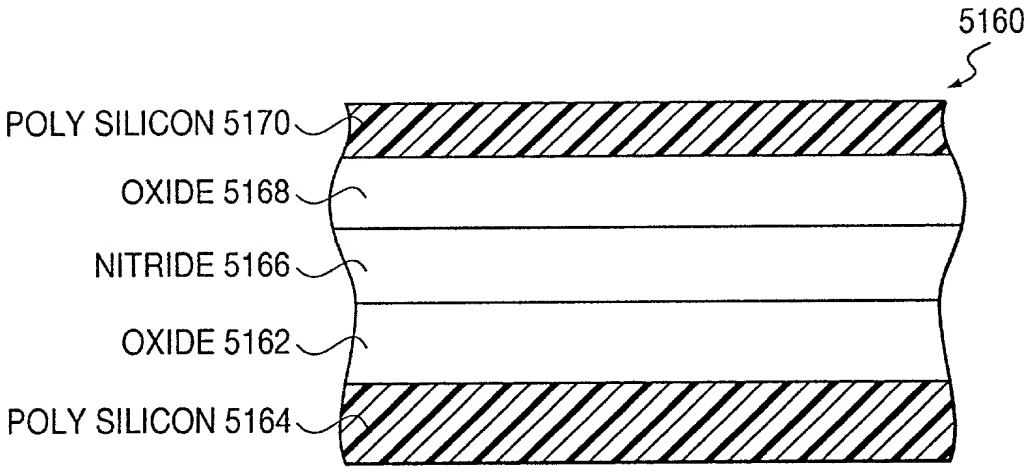

5160
POLY SILICON 5170
OXIDE 5168
NITRIDE 5166
OXIDE 5162
POLY SILICON 5164

FIG. 80

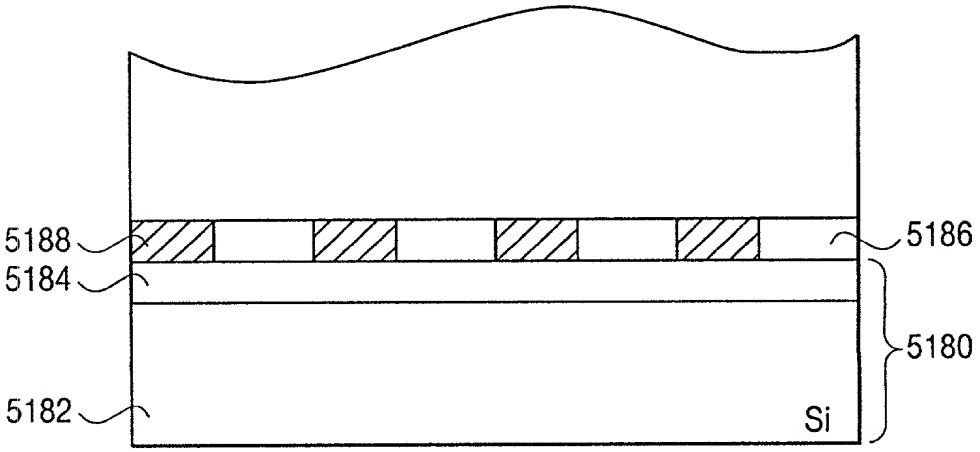

5188
5184
5182
5186
5180
Si

FIG. 78

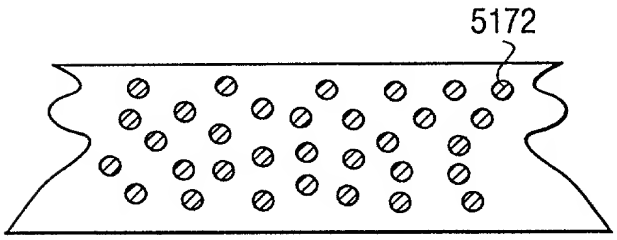


FIG. 79

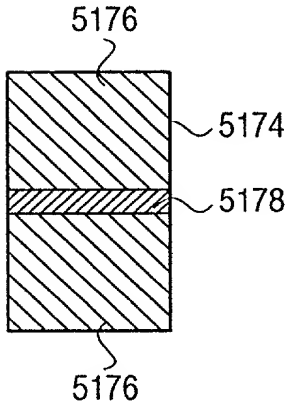


FIG. 81A

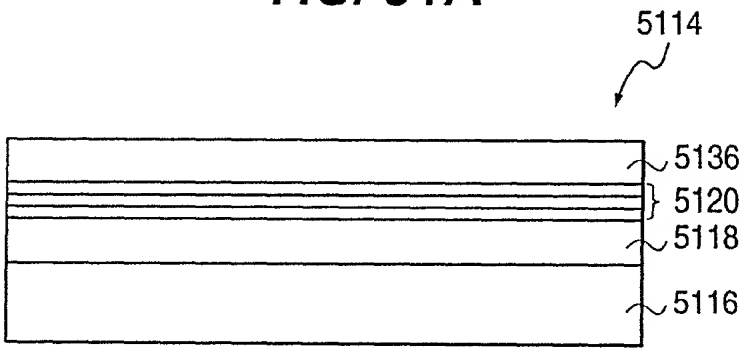


FIG. 81B

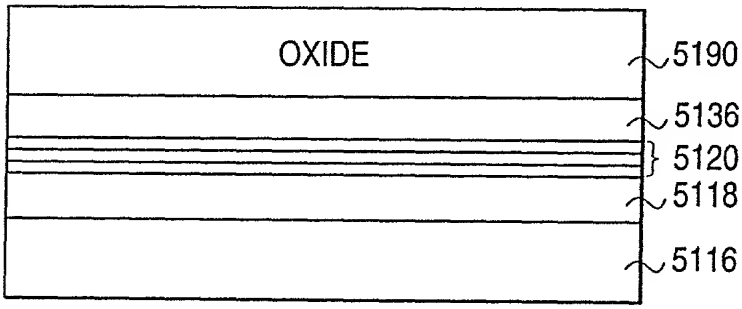


FIG. 81C

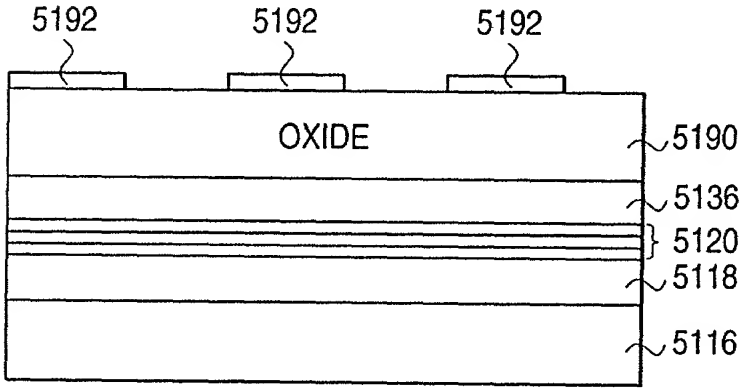


FIG. 81D

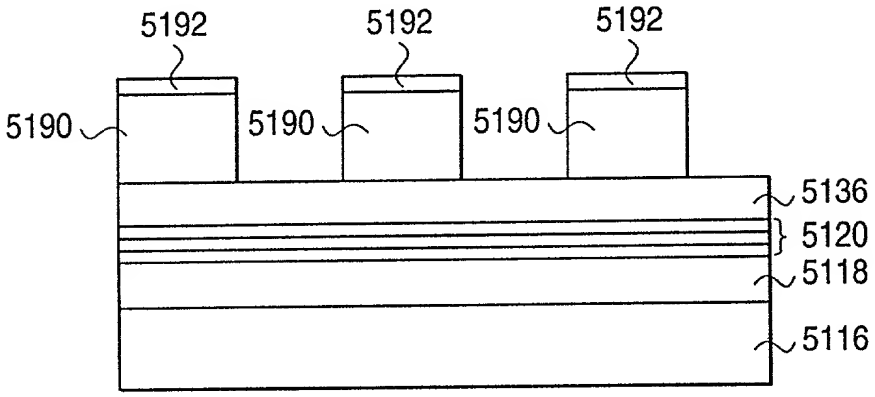


FIG. 81E

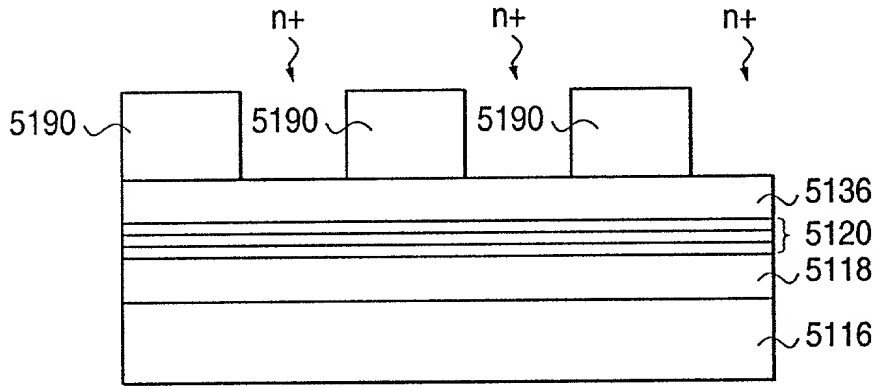


FIG. 81F

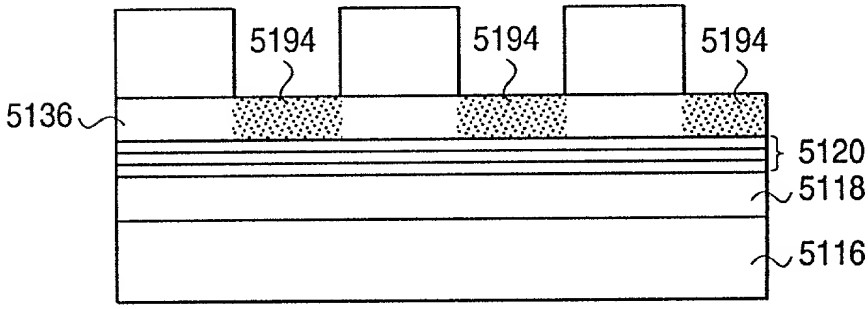


FIG. 81G

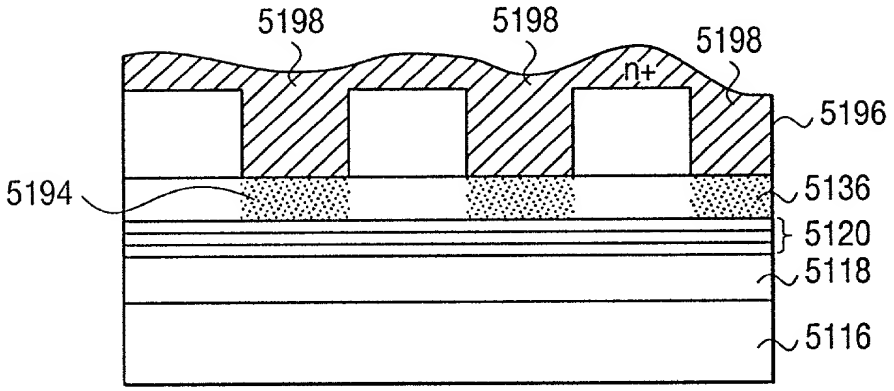


FIG. 81H

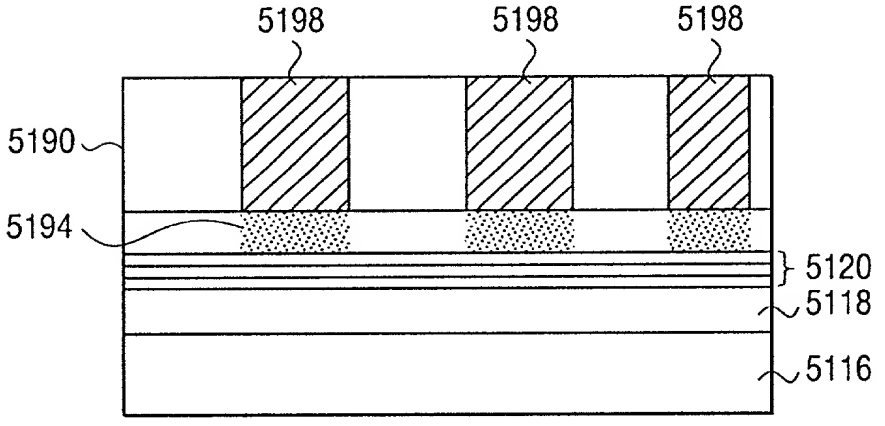


FIG. 82A

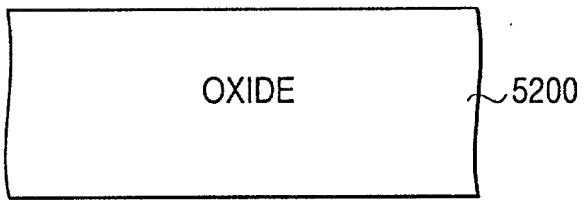


FIG. 82B

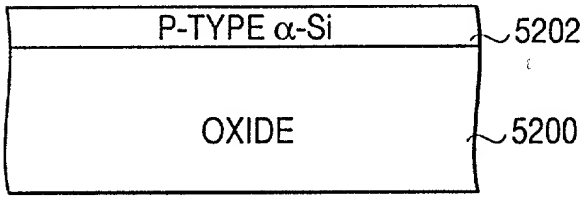


FIG. 82C

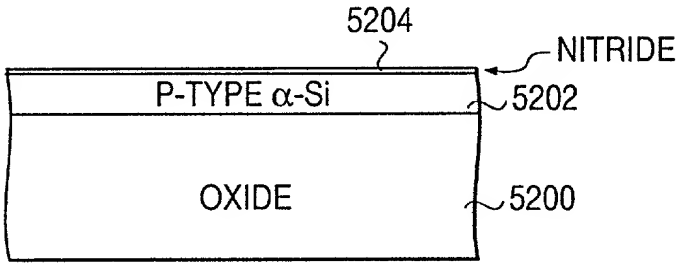


FIG. 82D

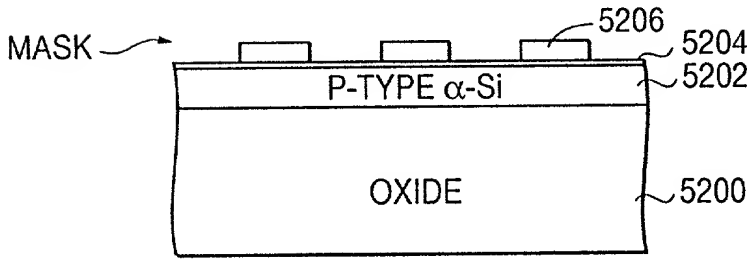


FIG. 82E

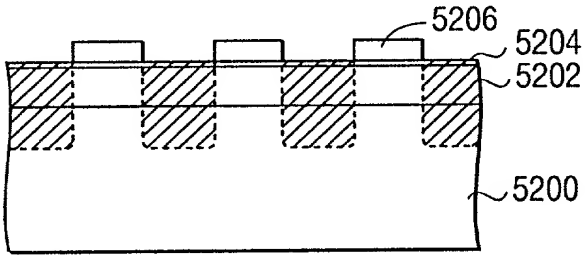


FIG. 82F

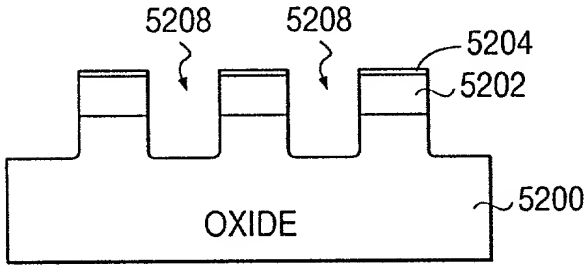


FIG. 82G

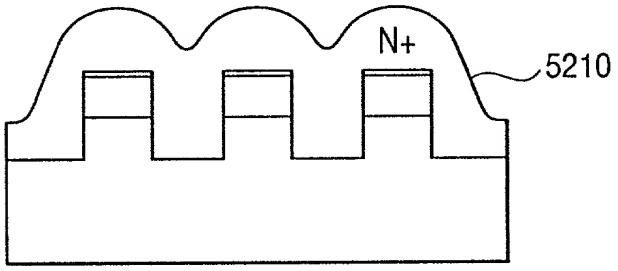


FIG. 82H

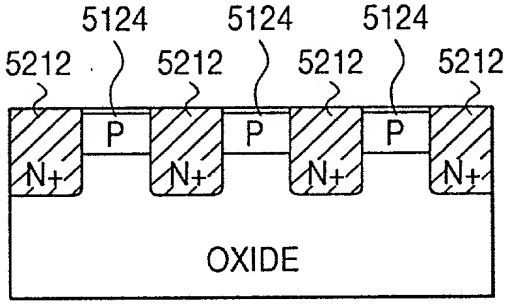


FIG. 82I

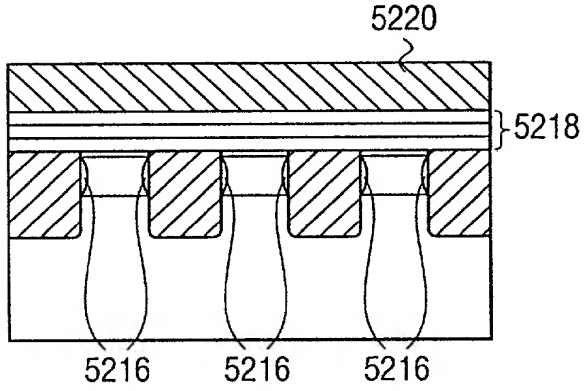


FIG. 83A

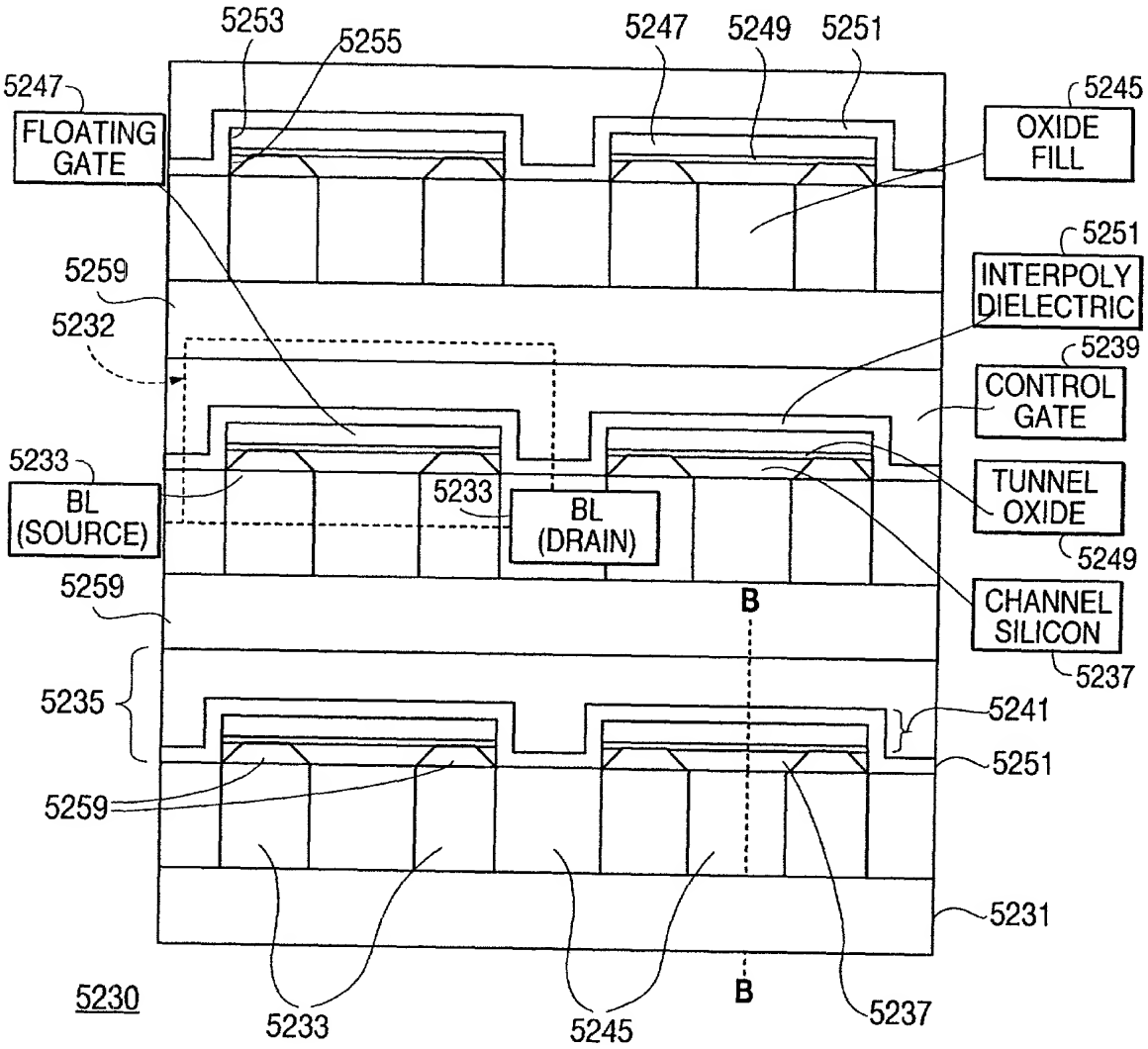

5253
5255
5247
5249
5251
5247
FLOATING GATE
5245
OXIDE FILL
5251
INTERPOLY DIELECTRIC
5259
5232
5239
CONTROL GATE
5233
BL (SOURCE)
5233
BL (DRAIN)
TUNNEL OXIDE
5249
5259
B
CHANNEL SILICON
5237
5235
5241
5251
5259
5231
5230
5233
5245
B
5237

FIG. 83B

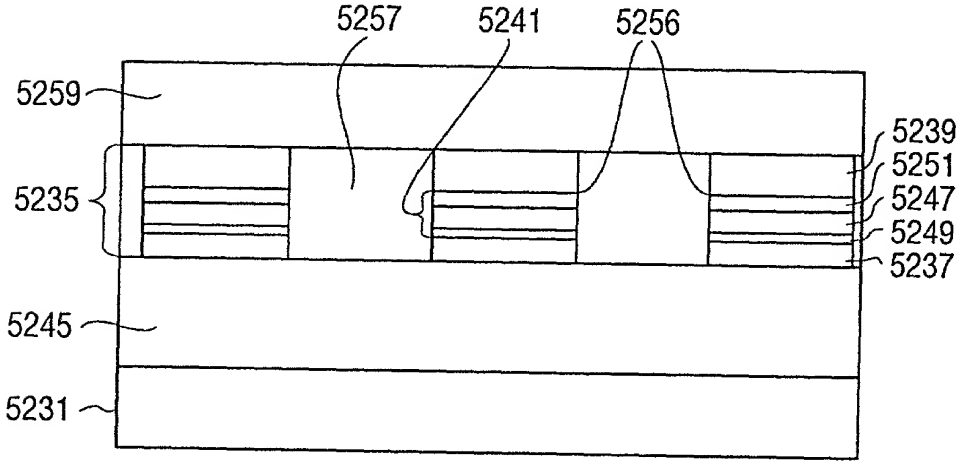


FIG. 84

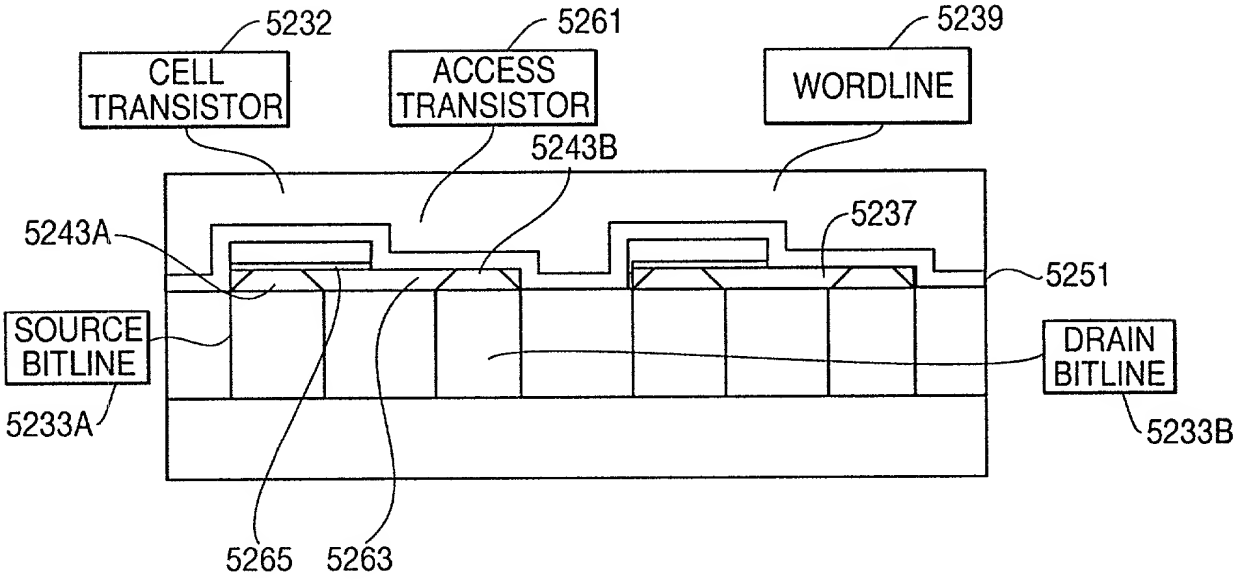

5232
CELL TRANSISTOR
5261
ACCESS TRANSISTOR
5239
WORDLINE
5243B
5243A
5237
5251
SOURCE BITLINE
DRAIN BITLINE
5233A
5233B
5265
5263

FIG. 85

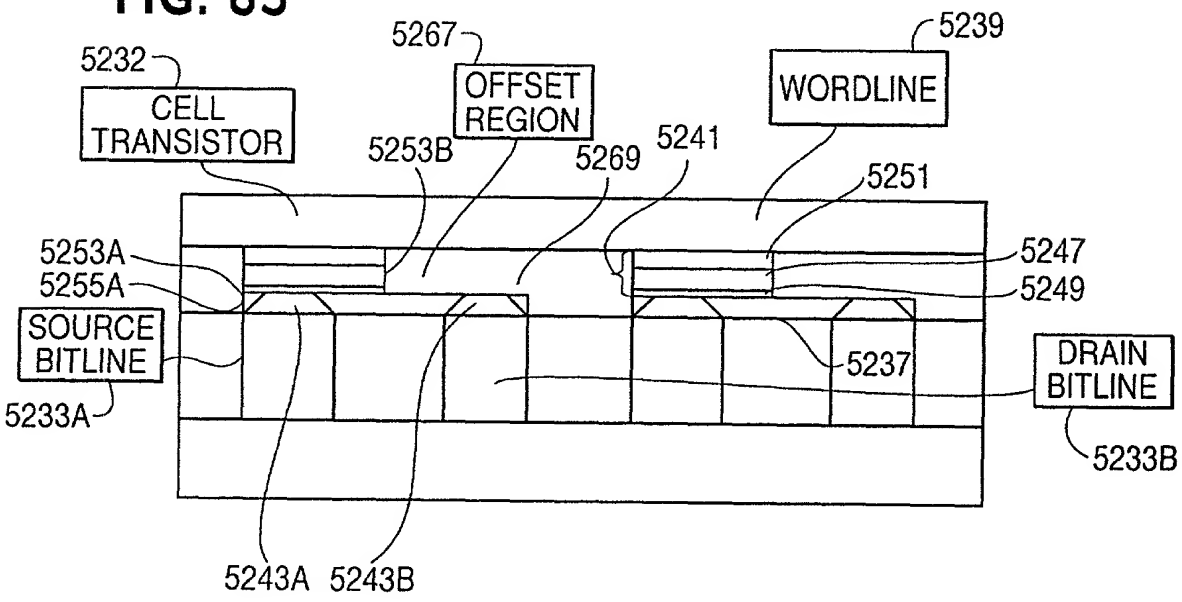

5232
CELL TRANSISTOR
5267
OFFSET REGION
5239
WORDLINE
5253B
5269
5241
5251
5253A
5255A
5247
5249
SOURCE BITLINE
5237
DRAIN BITLINE
5233A
5233B
5243A
5243B

FIG. 86A

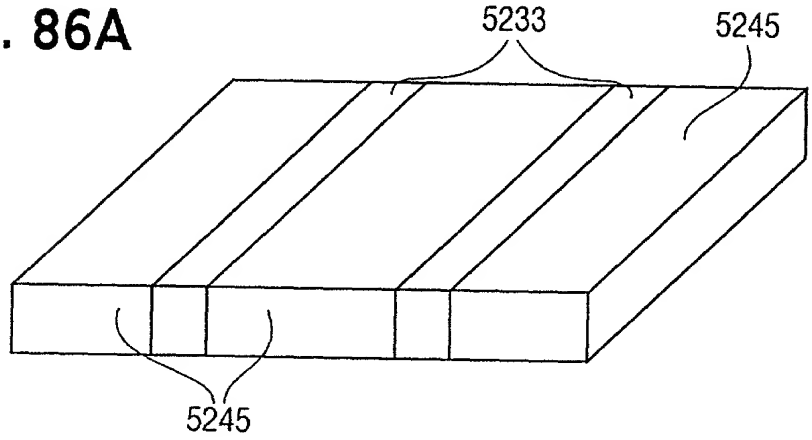


FIG. 86B

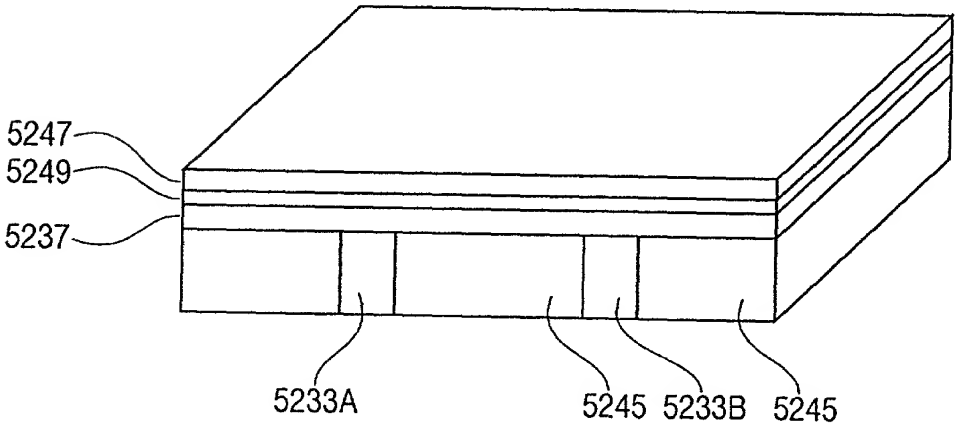


FIG. 86C

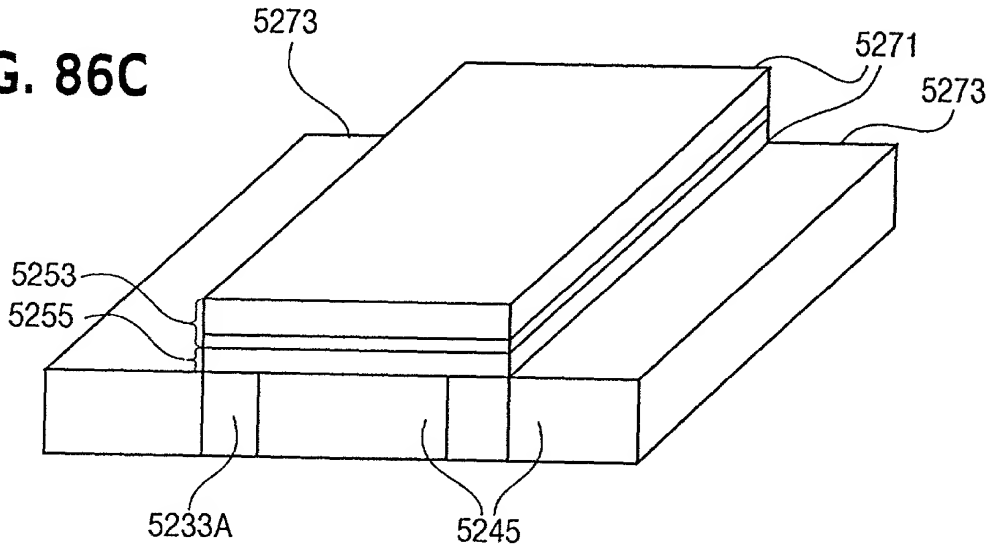


FIG. 86D

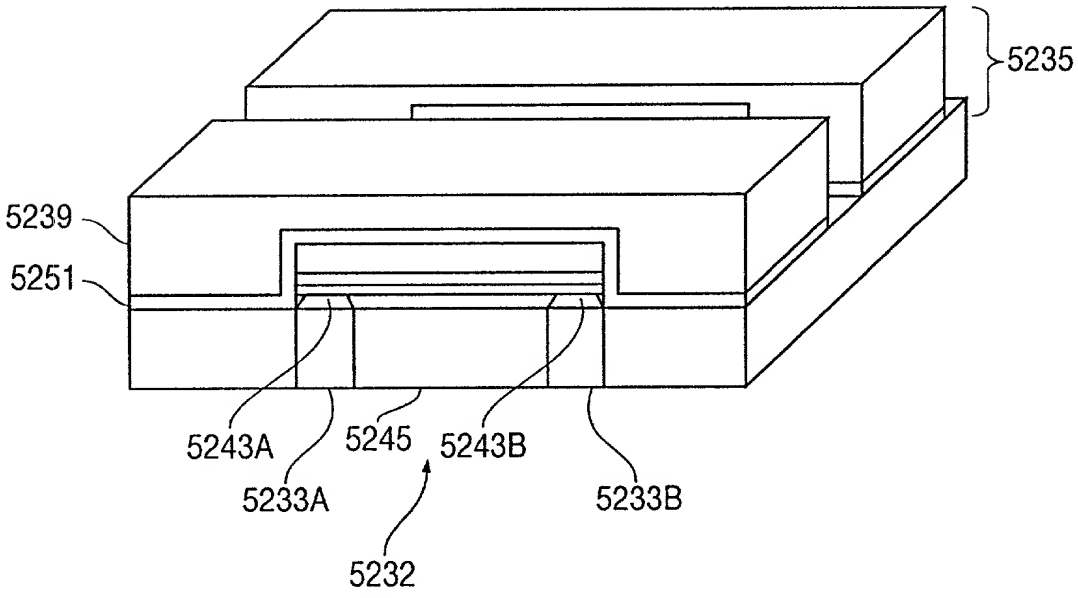


FIG. 86E

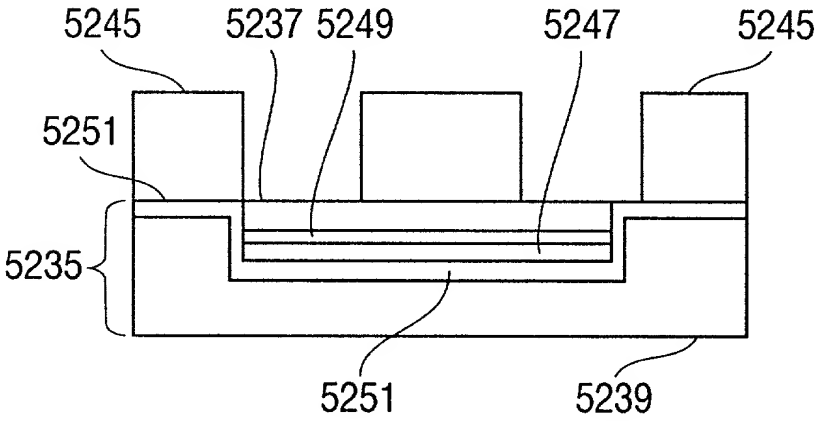


FIG. 86F

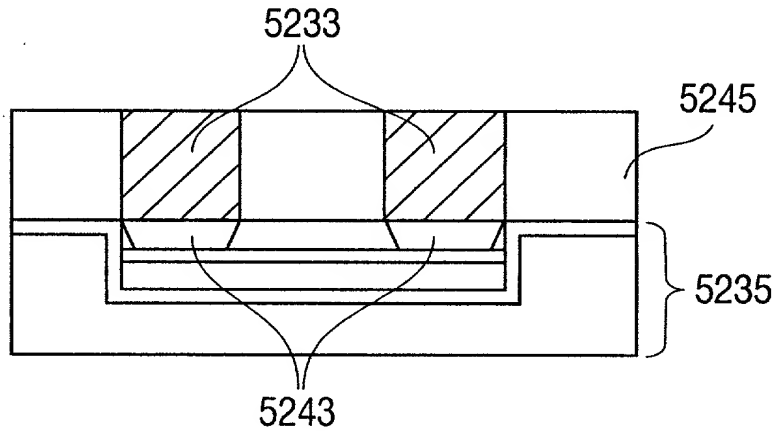


FIG. 86G

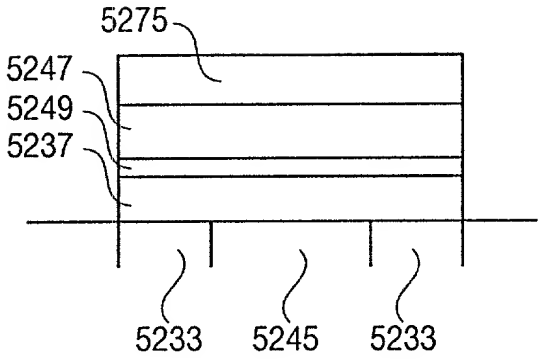


FIG. 86H

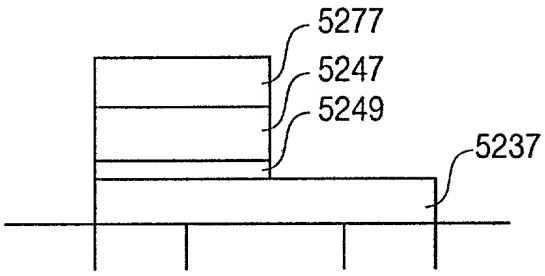


FIG. 86I

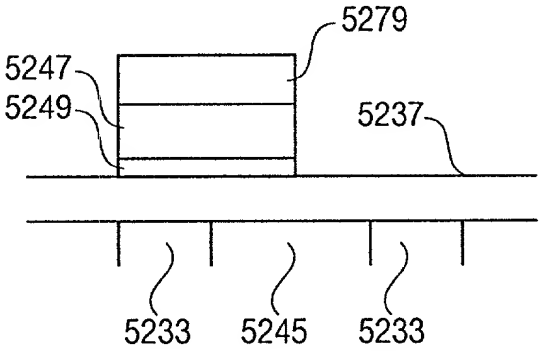
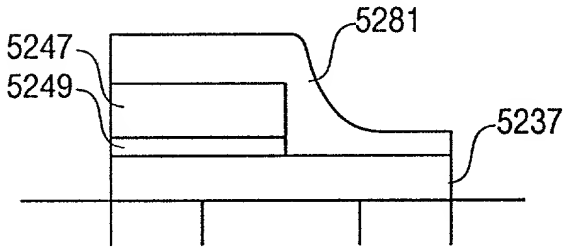


FIG. 86J



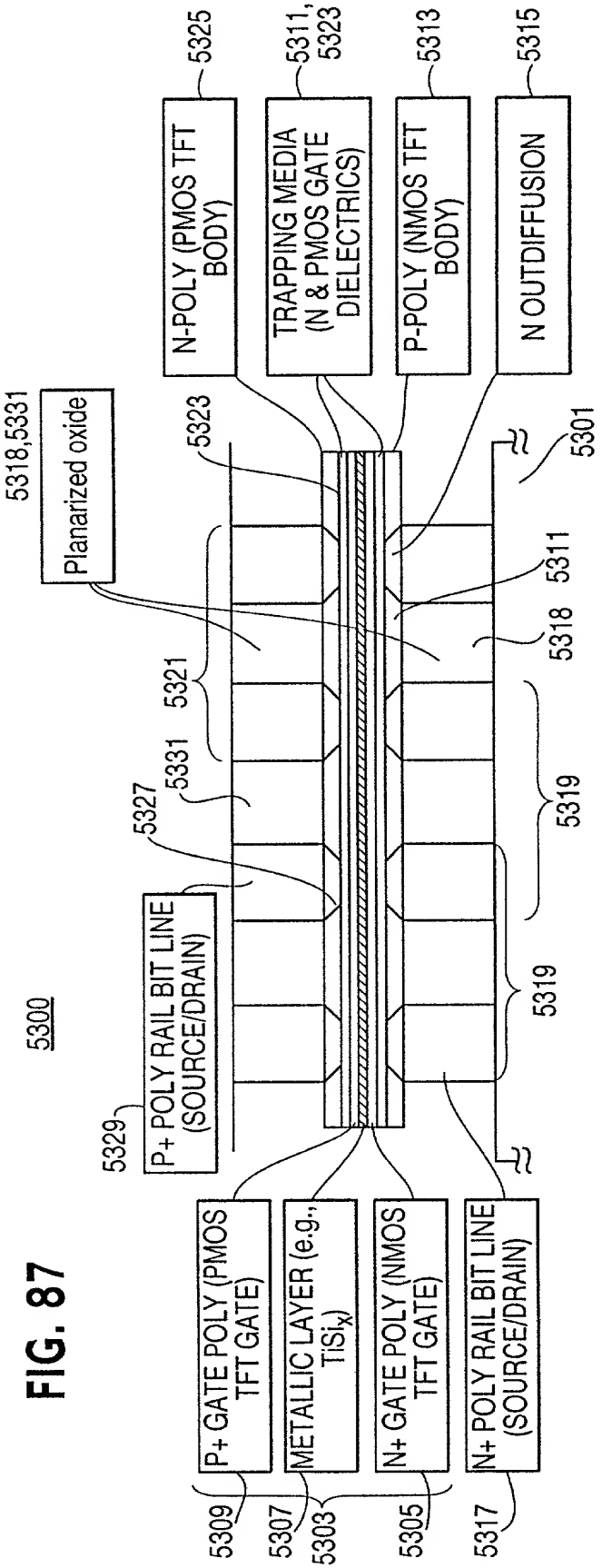

5300
5325
N-POLY (PMOS TFT BODY)
5311, 5323
TRAPPING MEDIA (N & PMOS GATE DIELECTRICS)
5313
P-POLY (NMOS TFT BODY)
5315
N OUTDIFFUSION
5318,5331
Planarized oxide
5323
5301
5311
5318
5321
5331
5327
5319
5319
P+ POLY RAIL BIT LINE (SOURCE/DRAIN)
5329
P+ GATE POLY (PMOS TFT GATE)
METALLIC LAYER (e.g., $TiSi_x$)
N+ GATE POLY (NMOS TFT GATE)
N+ POLY RAIL BIT LINE (SOURCE/DRAIN)
5309
5307
5303
5305
5317

FIG. 87

FIG. 88A

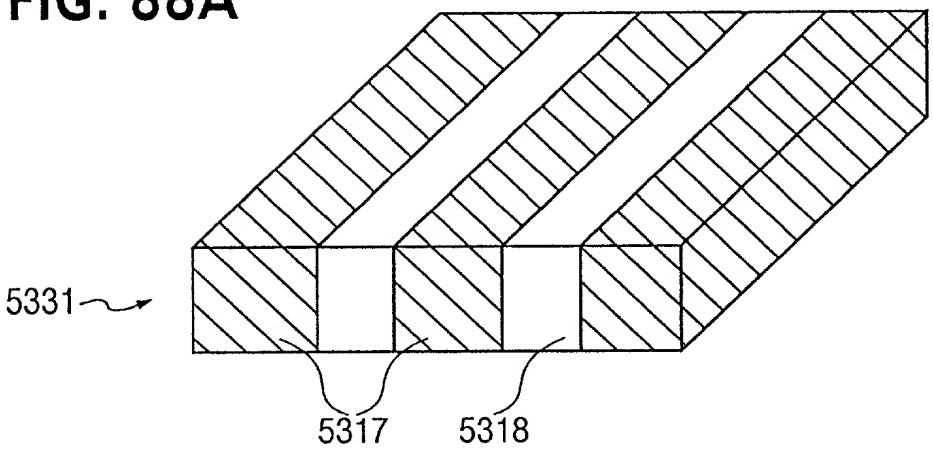


FIG. 88B

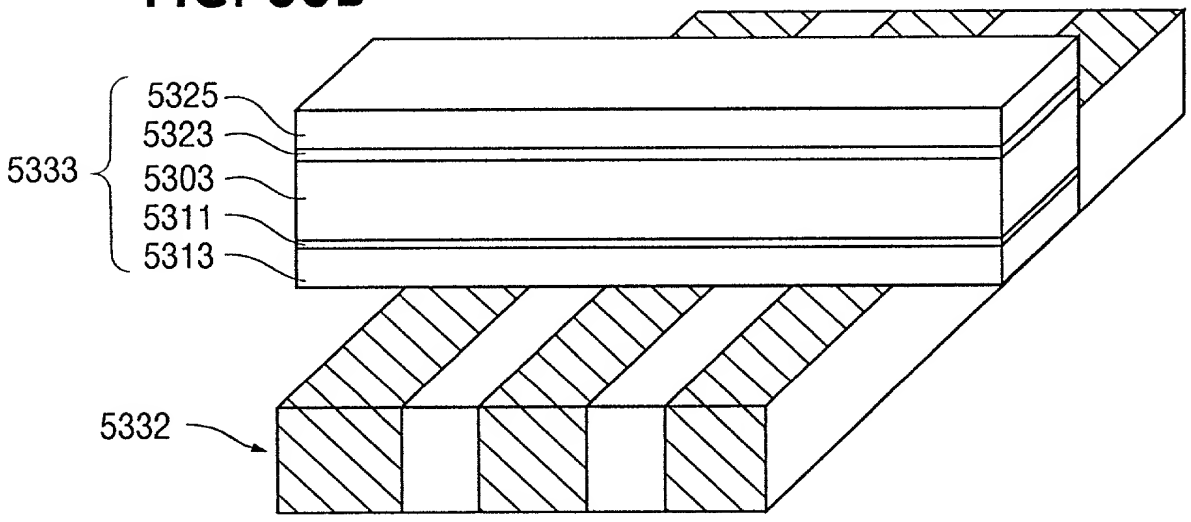


FIG. 88C

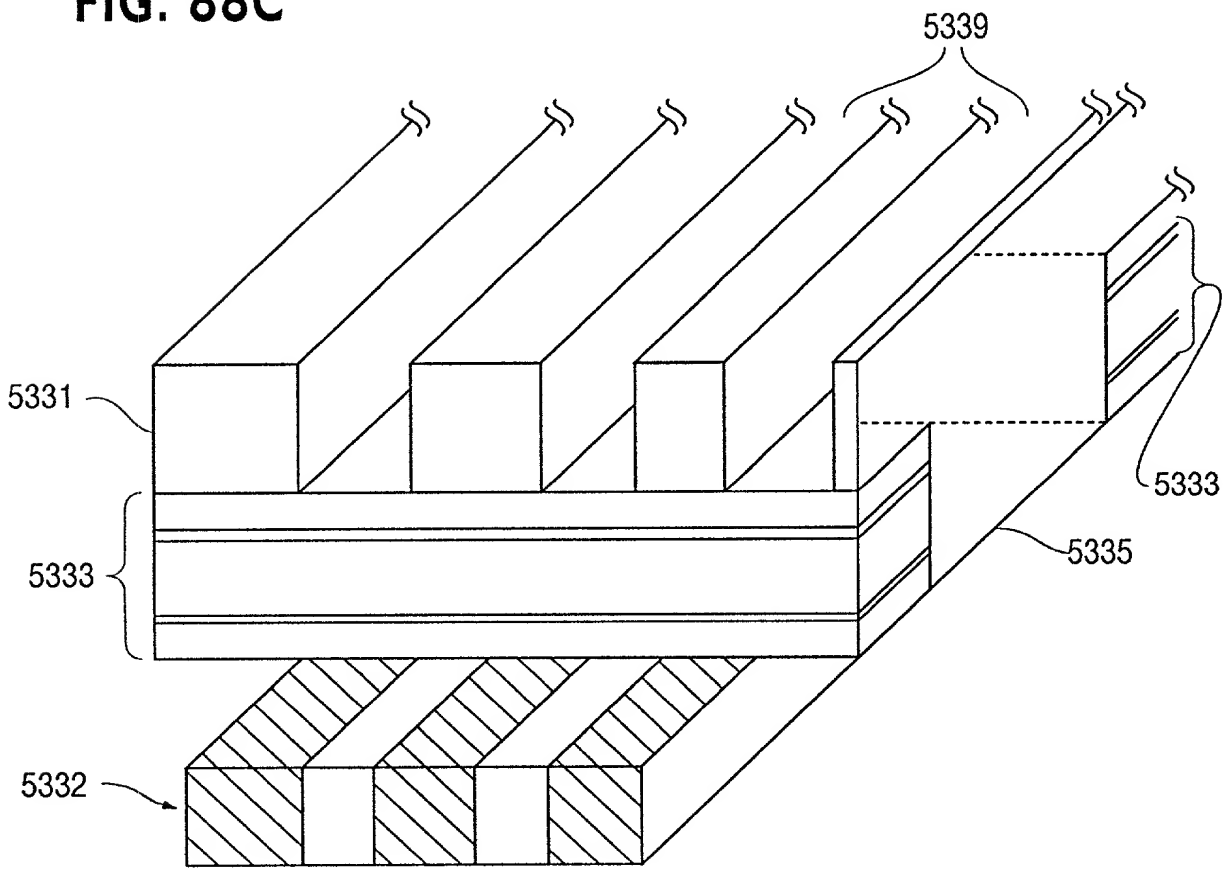


FIG. 88D

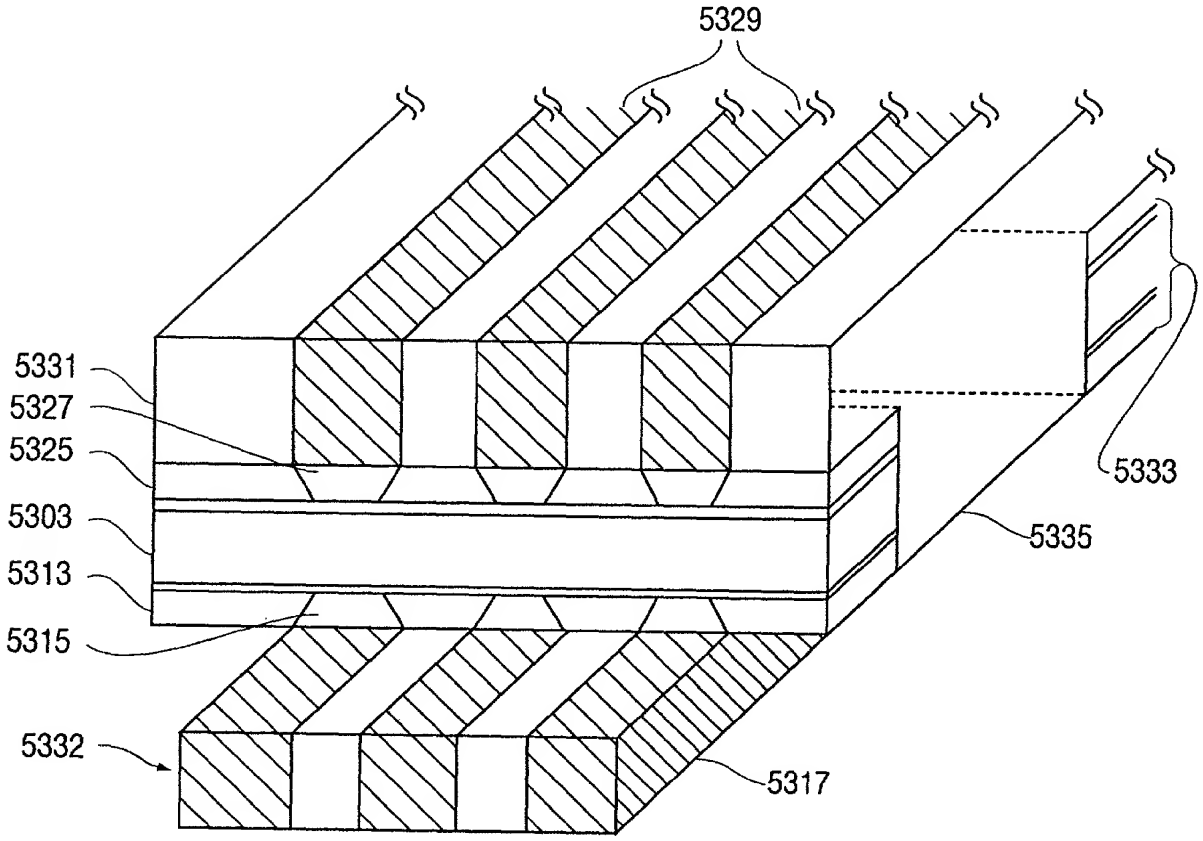


FIG. 89

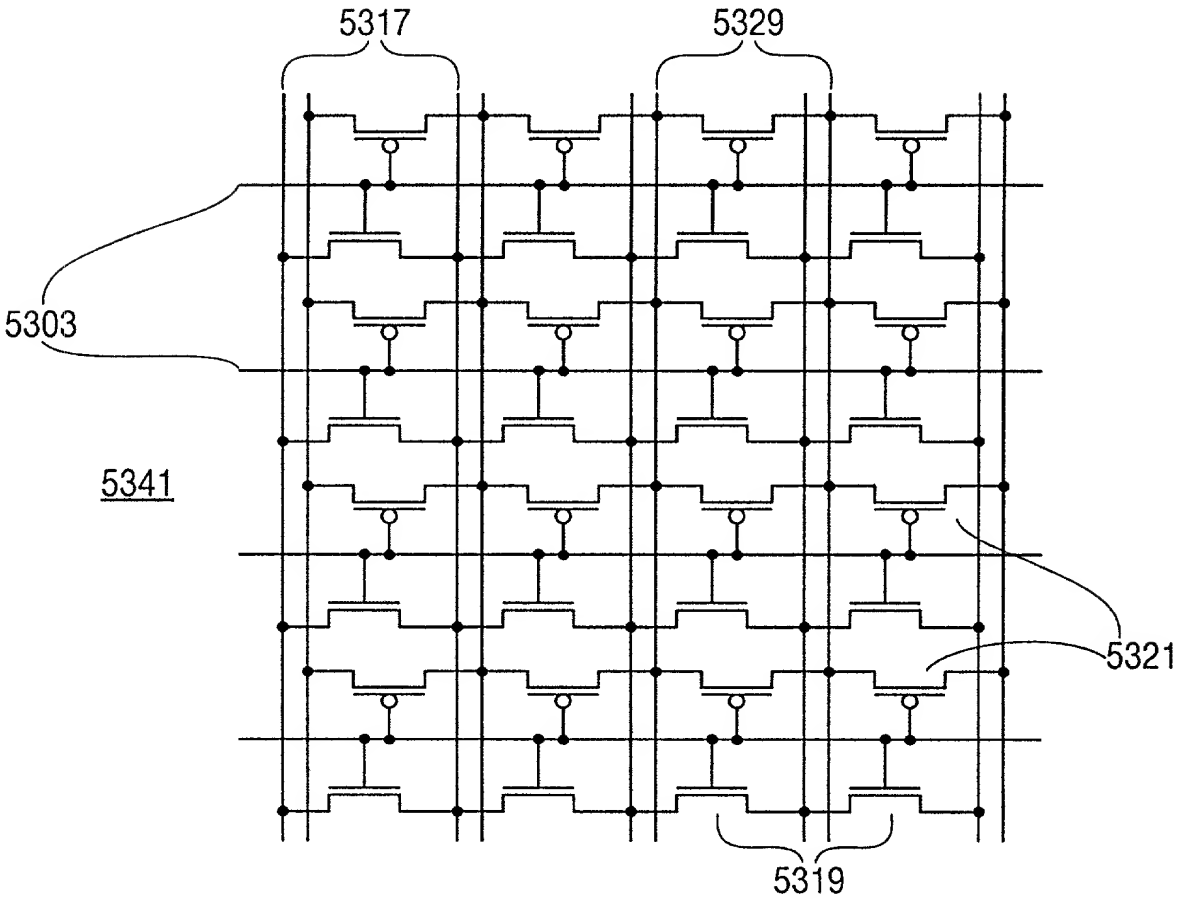


FIG. 90

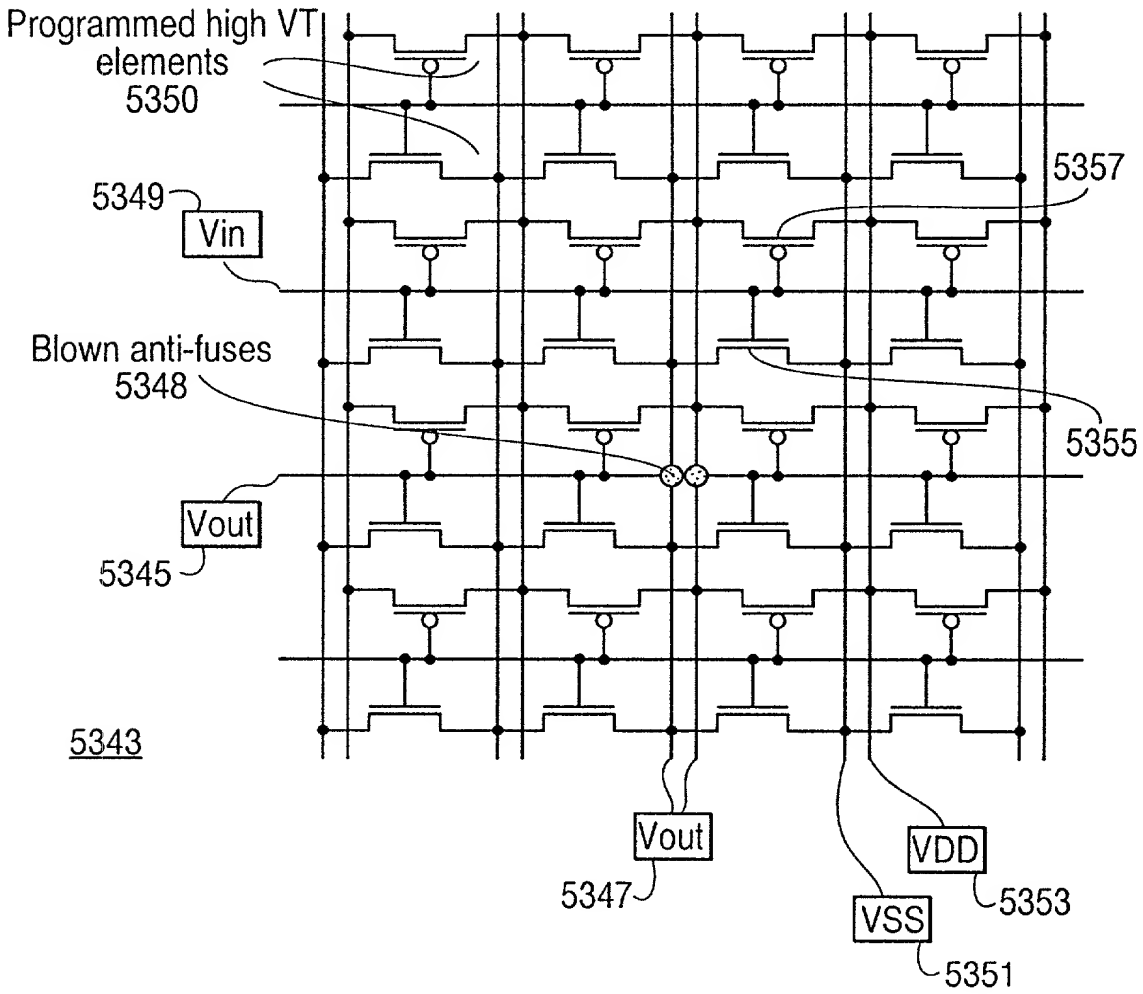

Programmed high VT elements 5350
5349
Vin
Blown anti-fuses 5348
Vout
5345
5343
5357
5355
Vout
5347
VDD
5353
VSS
5351

FIG. 91

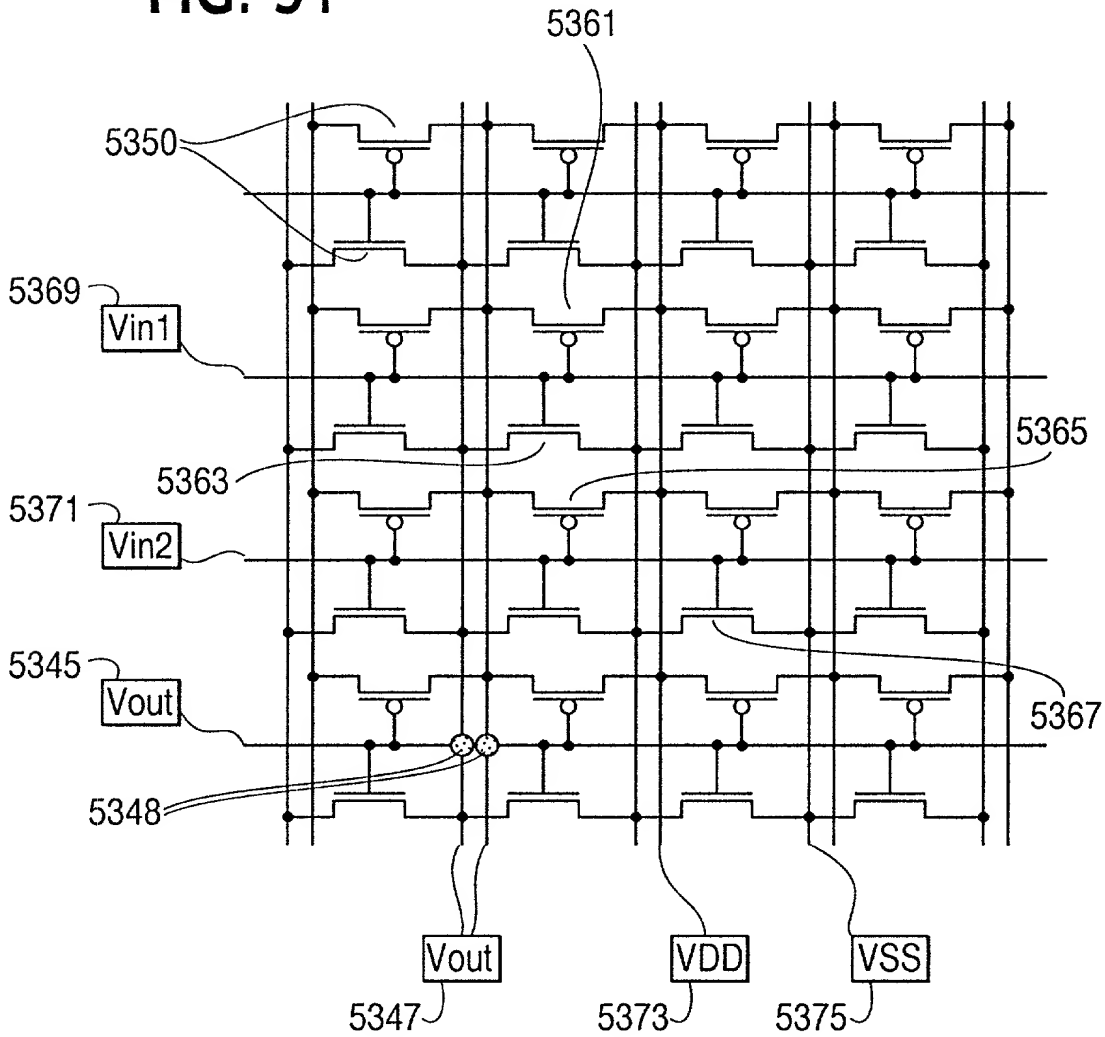

5361
5350
5369
Vin1
5365
5363
5371
Vin2
5345
Vout
5367
5348
Vout
VDD
VSS
5347
5373
5375

FIG. 92

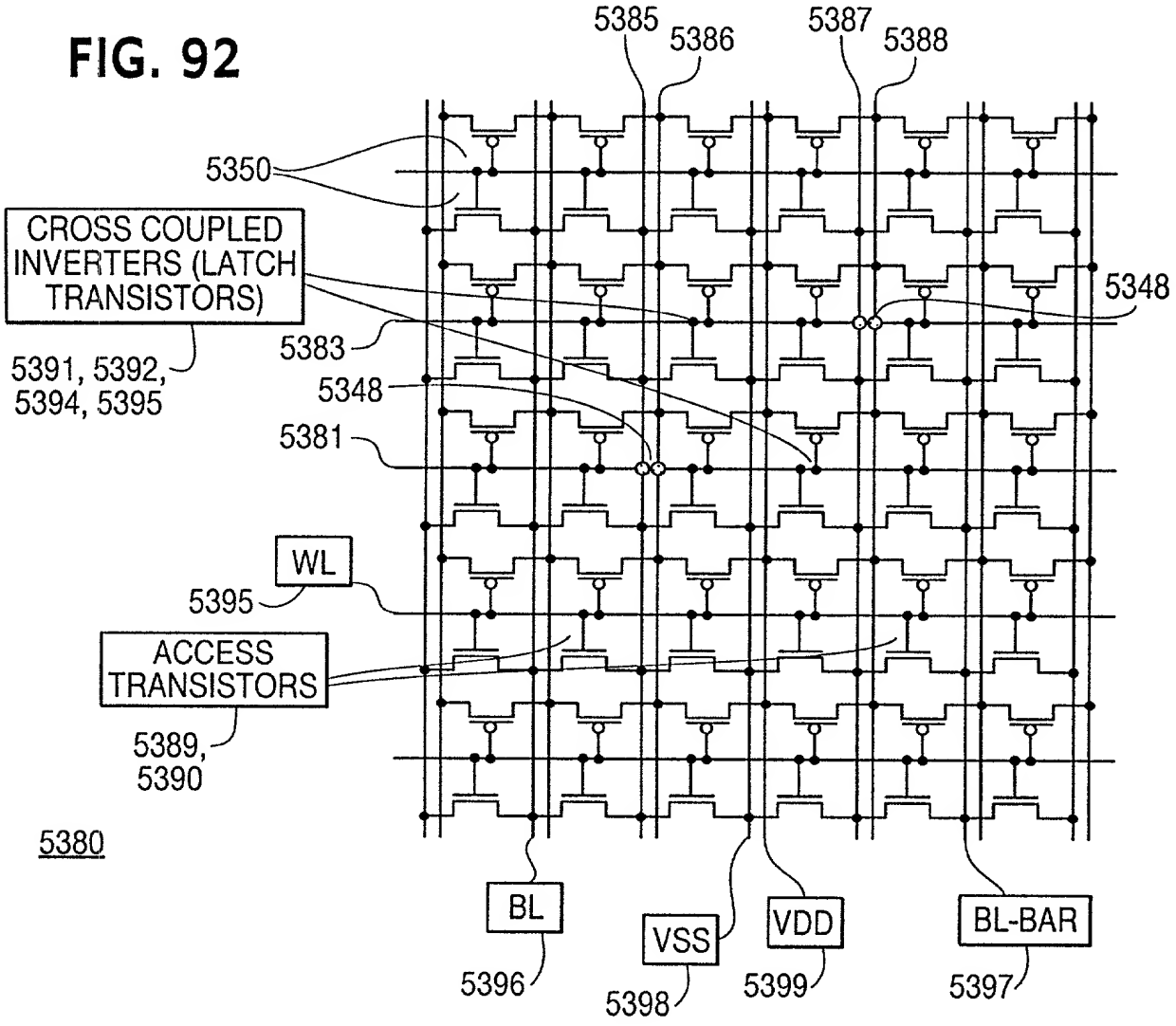

5385
5386
5387
5388
5350
CROSS COUPLED INVERTERS (LATCH TRANSISTORS)
5391, 5392, 5394, 5395
5348
5383
5348
5381
WL
5395
ACCESS TRANSISTORS
5389, 5390
5380
BL
VSS
VDD
BL-BAR
5396
5398
5399
5397

FIG. 93

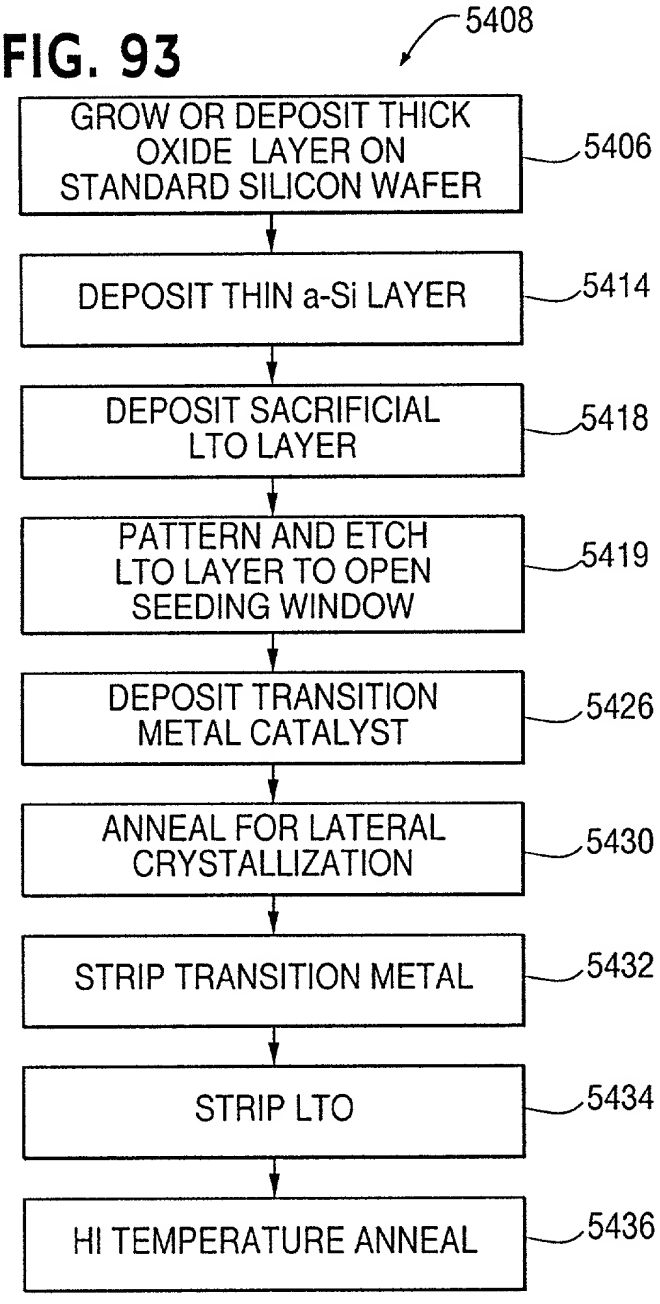

5408
GROW OR DEPOSIT THICK OXIDE LAYER ON STANDARD SILICON WAFER
5406
DEPOSIT THIN a-Si LAYER
5414
DEPOSIT SACRIFICIAL LTO LAYER
5418
PATTERN AND ETCH LTO LAYER TO OPEN SEEDING WINDOW
5419
DEPOSIT TRANSITION METAL CATALYST
5426
ANNEAL FOR LATERAL CRYSTALLIZATION
5430
STRIP TRANSITION METAL
5432
STRIP LTO
5434
HI TEMPERATURE ANNEAL
5436

FIG. 94A

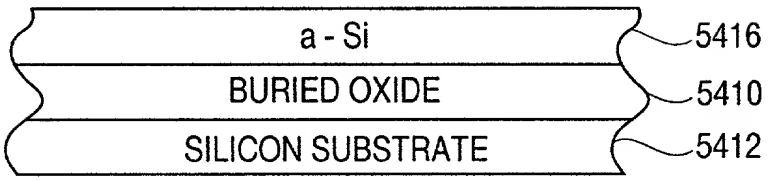


FIG. 94B

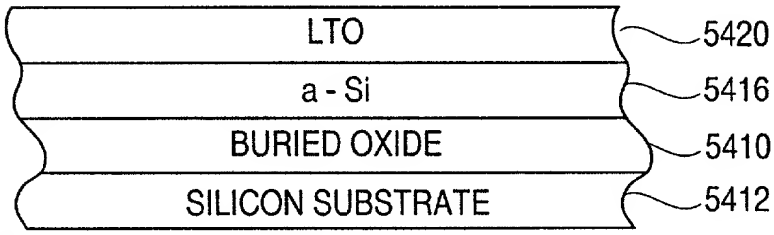


FIG. 94C

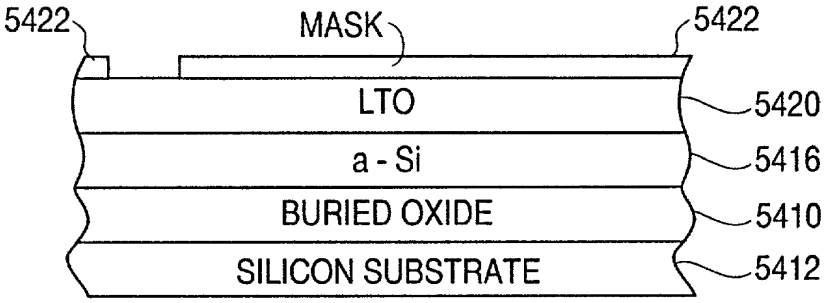


FIG. 94D

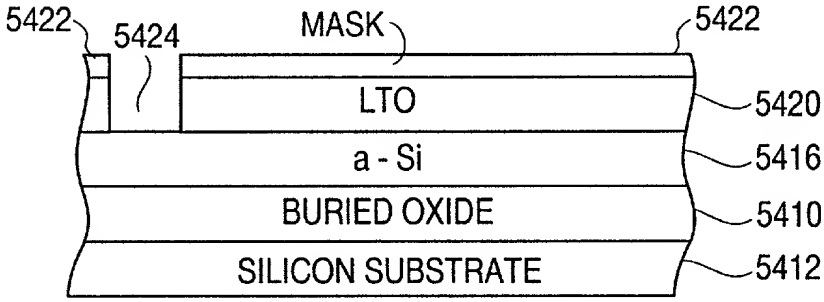


FIG. 94E

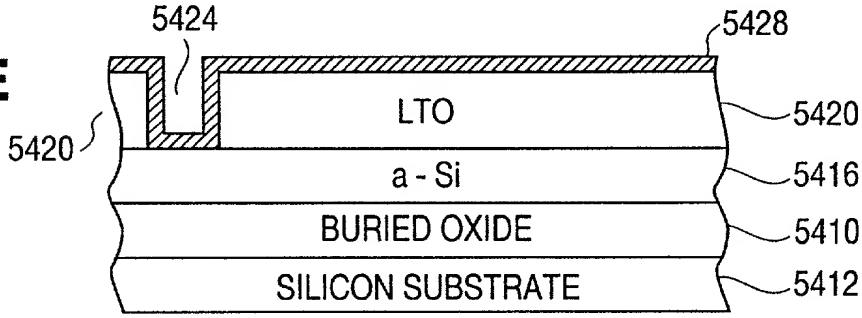


FIG. 94F

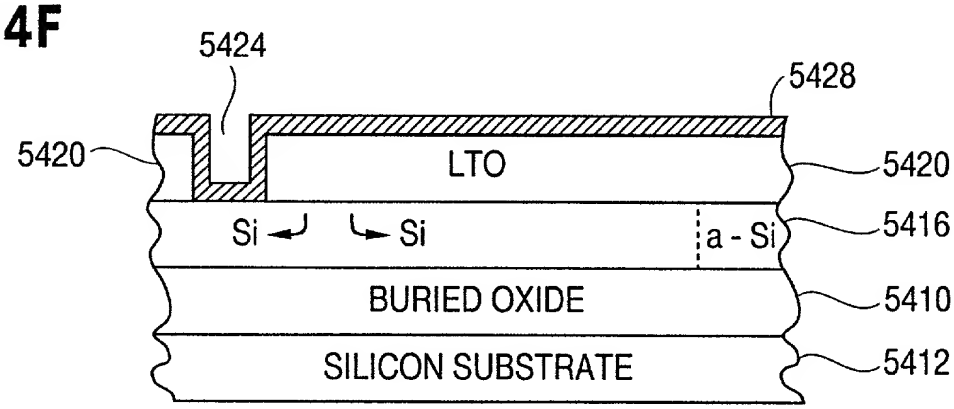


FIG. 94G

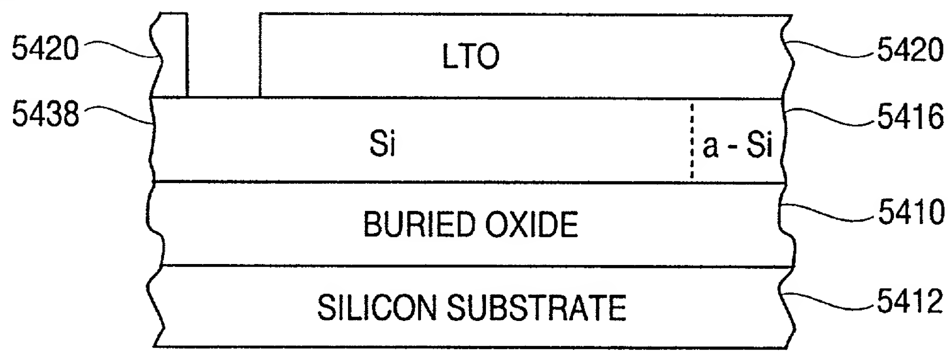


FIG. 94H

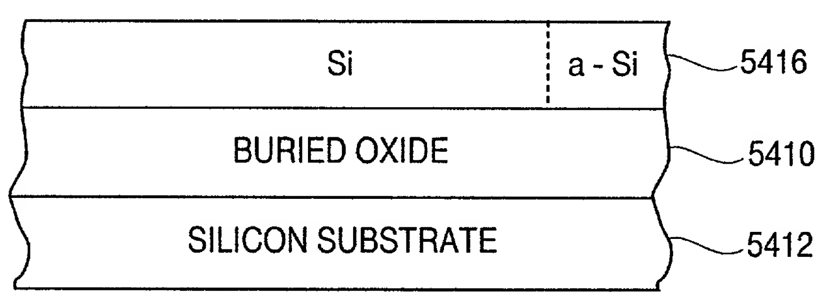


FIG. 95

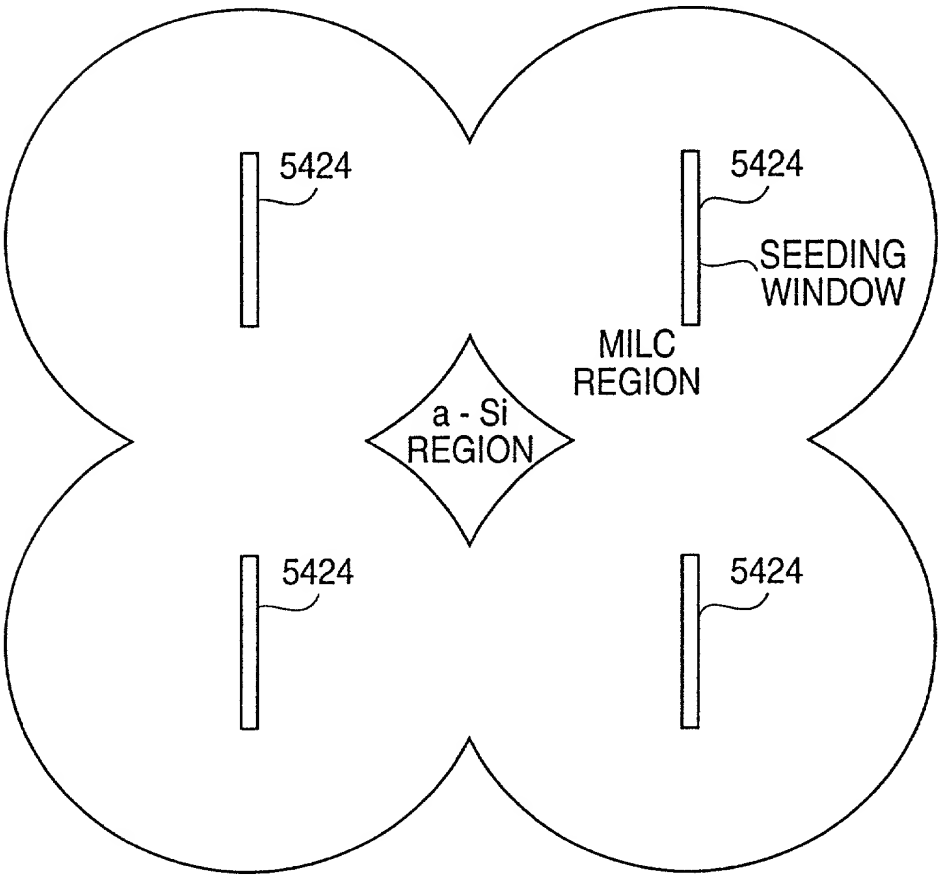


FIG. 96
(PRIOR ART)

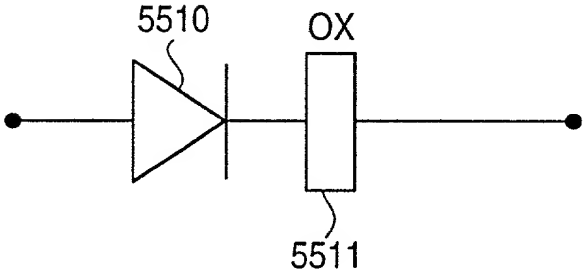
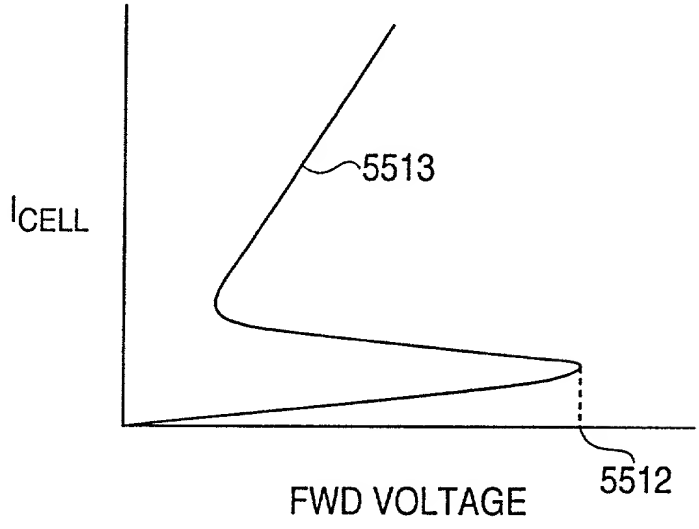


FIG. 97
(PRIOR ART)



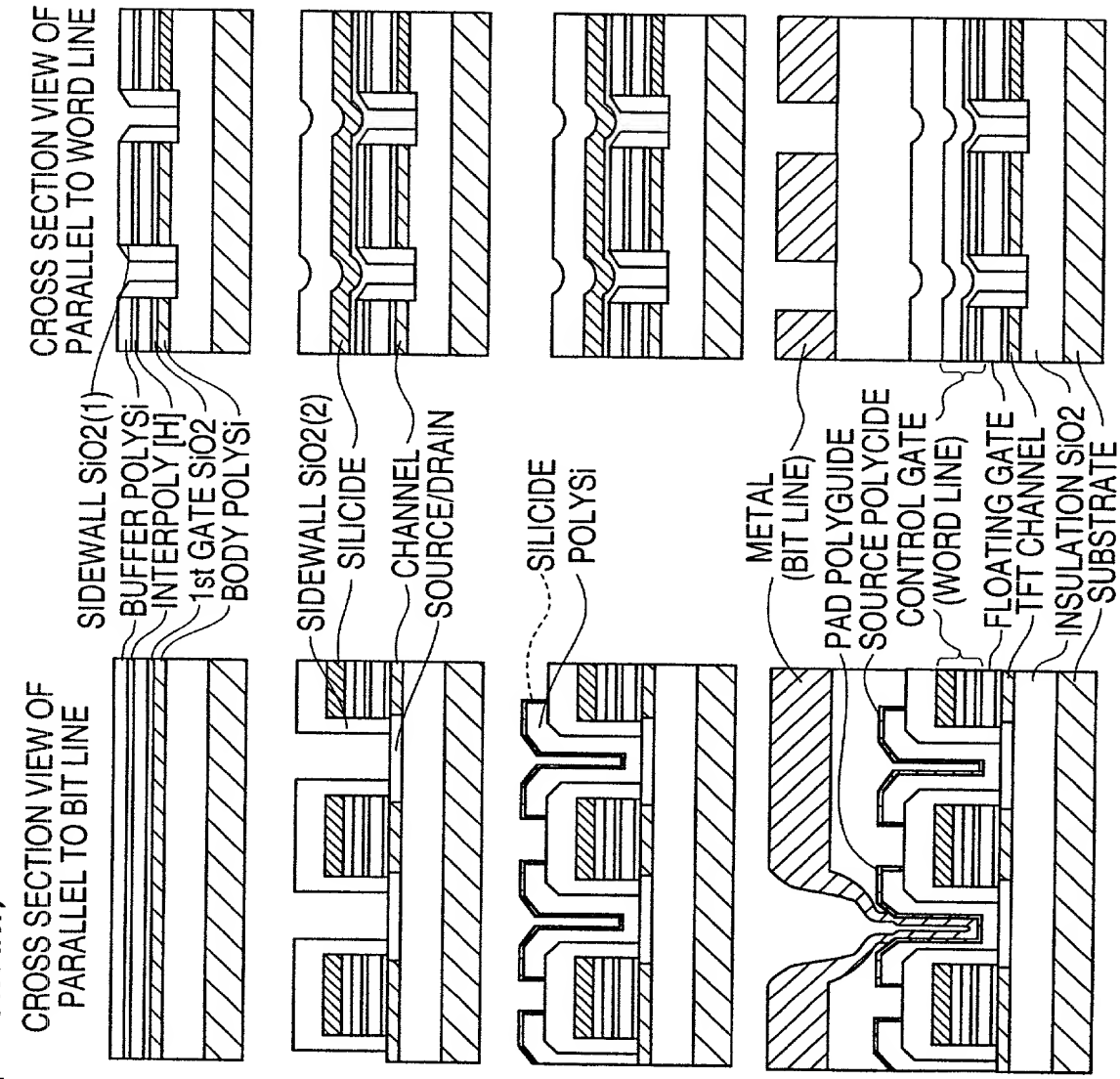


FIG. 98
(PRIOR ART)

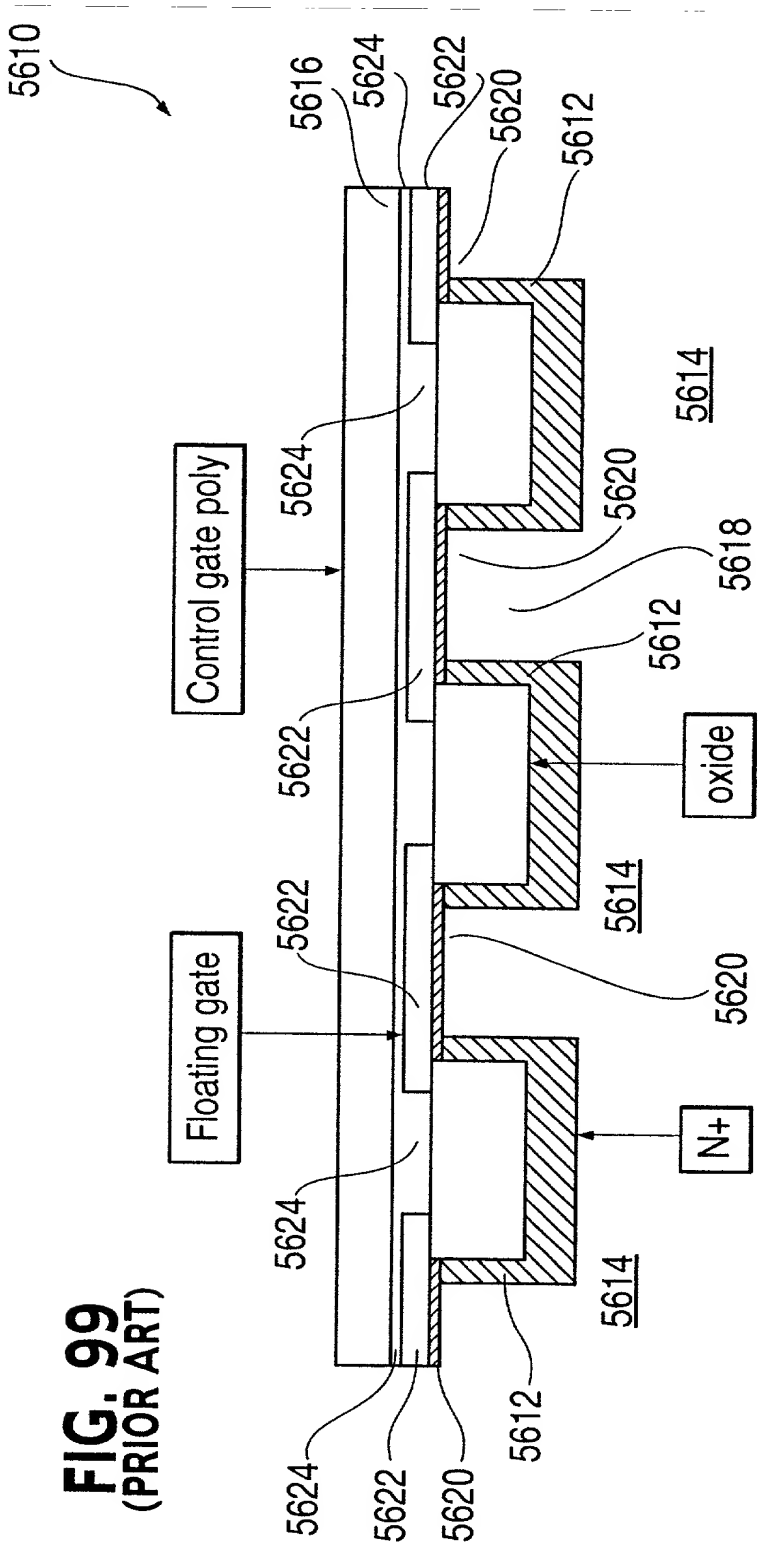


FIG. 99
(PRIOR ART)

FIG. 100
(PRIOR ART)

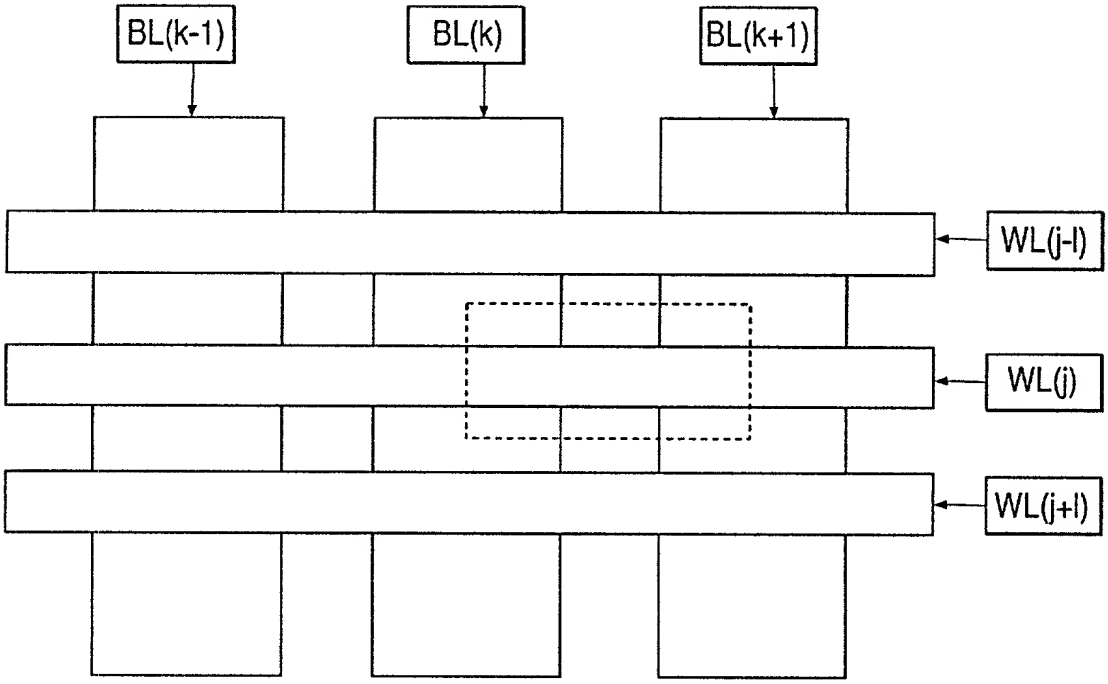


FIG. 101
(PRIOR ART)